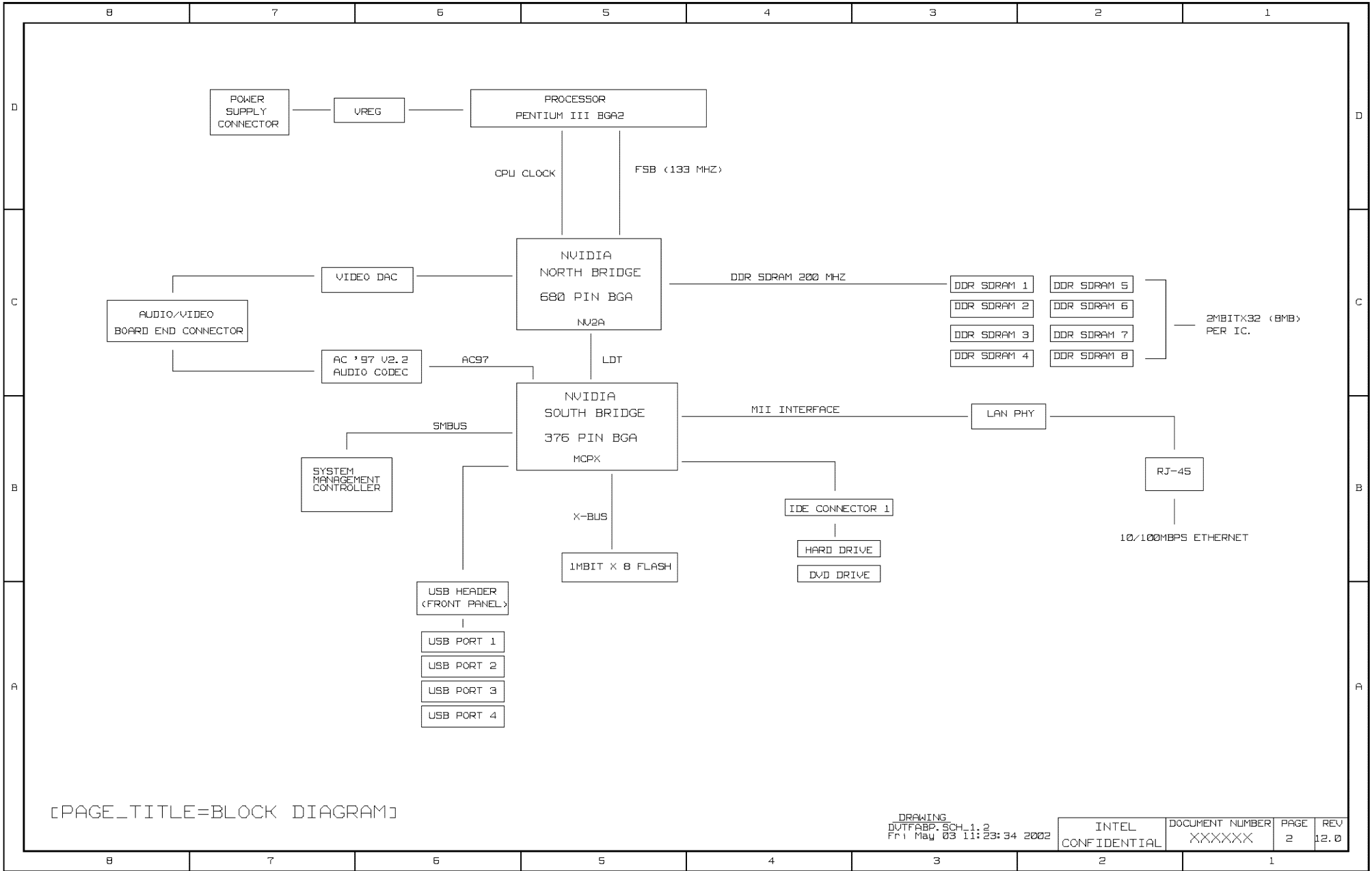
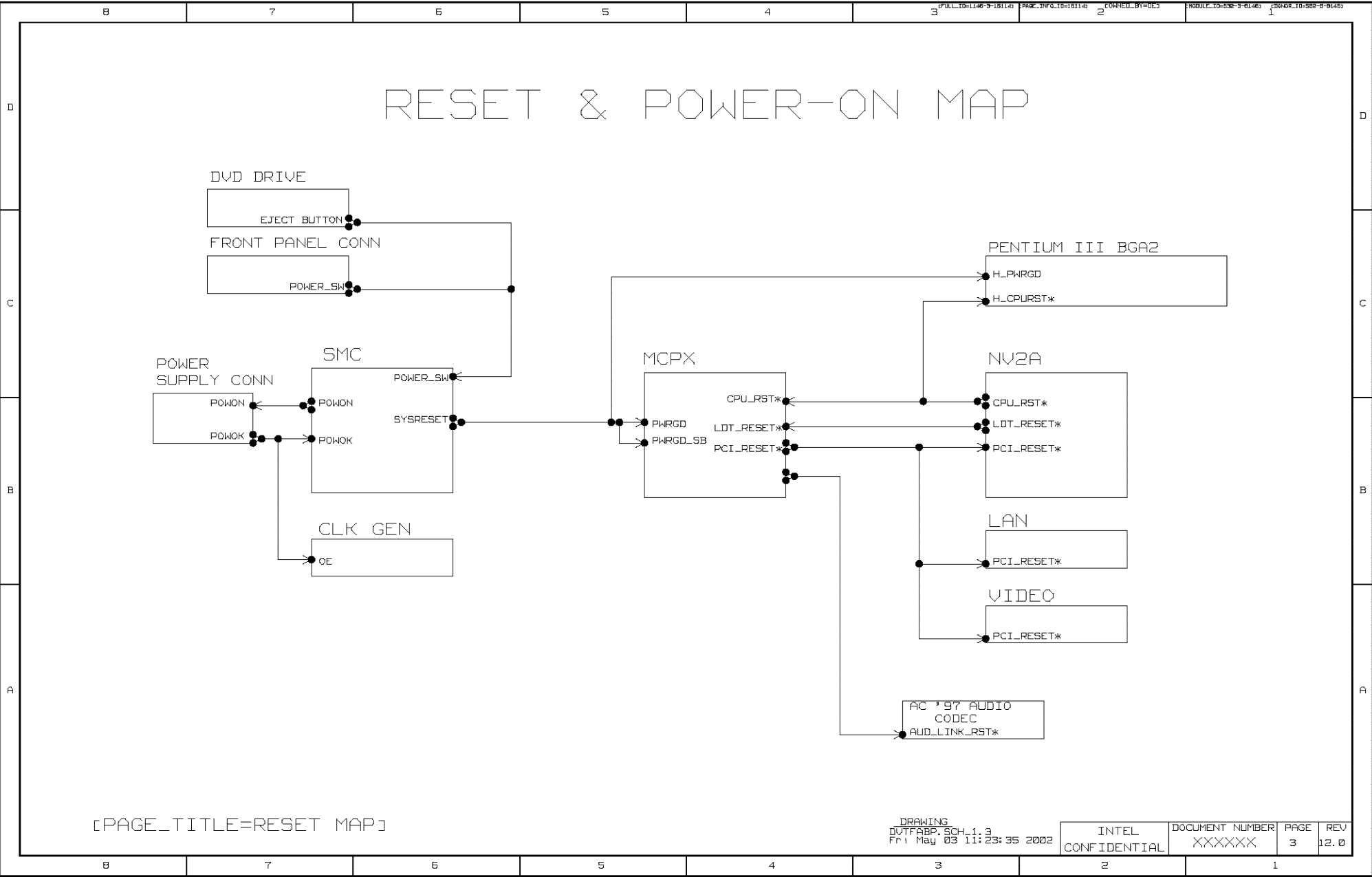


8		7		6		5		4		3		2		1					
										SCHEMATIC REV 12.0		PBA NUMBER P88754-300		REV 01		BOM RELEASE DATE 04/26/02			
PAGE										PAGE									
CONTENTS										CONTENTS									
[1] COVER PAGE]										[27] CPU VREG OUTPUT FILTER]		DVT REV 12.0 FAB P STANDARD BOM: MICRON DDR SEE PAGE 13 FOR SAMSUNG ALT XBLADE							
[2] BLOCK DIAGRAM]										[28] 1.5V SWITCHING REGULATOR]									
[3] RESET MAP]										[29] CLOCK GENERATOR]									
[4] GPIO/IDSEL TABLE]										[30] 1.25V LINEAR REGULATOR]									
[5] PENTIUM III BGA2 PART 1 OF 4]										[31] LINEAR_REGULATORS_1.5_2.5]									
[6] PENTIUM III BGA2 PART 2 OF 4]										[32] DVT POWER CONNECTOR]									
[7] PENTIUM III BGA2 PARTS 3 & 4]										[33] BULK DECOUPLING]									
[8] CPU VCORE DECOUPLING]										[34] SUPERCAP VBAT REGULATOR]									
[9] CPU VTT DECOUPLING]										[35] LAN ICS1893]									
[10] ITP TERMINATION]										[36] LAN JACK/THERMAL SENSE/EEPROM]									
[11] NV2A 1 OF 2(NORTH BRIDGE)]										[37] IDE]									
[12] NV2A 2 OF 2(NORTH BRIDGE)]										[38] AUDIO CODEC]									
[13] NV2A STRAPPING]										[39] AUDIO AMPLIFIER]									
[14] DDR SDRAM (PARTITION A)]										[40] AUDIO VREG AND BIAS]									
[15] DDR SDRAM (PARTITION B)]										[41] CX25871\SAN ANTONIO VIDEO-ENCODER]									
[16] DDR SDRAM (PARTITION C)]										[42] CX25874 VIDEO DAC AND TV ENCODER]									
[17] DDR SDRAM (PARTITION D)]										[43] VIDEO DAC AND TV ENCODER]									
[18] DDR PARALLEL TERM DATA A/B]										[44] AV CONNECTOR]									
[19] DDR PARALLEL TERM DATA C/D]										[45] LABELS AND MOUNTING HOLES]									
[20] VTERM DECOUPLING]										[46] FLASH]									
[21] MEMORY DECOUPLING]										[47] USB FRONT PANEL]									
[22] NV2A DECOUPLING]										[48] NV2A FAN/5V DRAIN/BROWN OUT]									
[23] MCPX 1 OF 2]										[49] SMC/FAN/DVD PWR/FRONT PANEL]									
[24] MCPX 2 OF 2]										[50] MCPX MUXED PIN ASSIGNMENT]									
[25] MCPX INPUT STRAPS]										[51-56] INDEX]									
[26] CPU VOLTAGE REGULATOR]																			
NOTES:																			
1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.																			
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.																			
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.																			
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.																			
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.																			
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.																			
[PAGE_TITLE=COVER PAGE]																			
DRAWING DVT/FABP_SCH.1.1 Fri May 03 11:23:32 2002																			
BOM RELEASE DATE										10X/10X/10X		PB NUMBER		XXXXXX-XXX					
SIGNATURE										DATE		intel		3055 BOWERS AVE SANTA CLARA, CA 95051					
DRN BY												TITLE							
CHK BY										1000000		10X/10X/10X		SCH, PBA, XBLADE					
EPL																			
APVD												INTEL		DOCUMENT NUMBER		PAGE		REV	
APVD												CONFIDENTIAL		XXXXXX		1/56		12.0	
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PCI DEVICE MAP

DEVICE	PCI BUS #	DEVICE #	FUNCTION	DEVICE ID	COMMENTS
NV2A					
HOST BRIDGE	00	00	00	02A8	IT IS DIFFERENT FUNCTIONALLY FROM CRUSH12
AGP BRIDGE	00	30	00	01B7	SECONDARY BRIDGE #=1 IN STD ENUMERATION
NV2A	02	00	00	02A0	
MCPX					
APU	00	05	00	01B0	
AUDIO CODEC	00	06	00	01B1	
USB1.1 OHCI A	00	02	00	01C2	
USB1.1 OHCI B	00	03	00	01C2	
HAC	00	04	00	01C3	
IDE	00	09	00	01BC	
SMBUS2	00	01	01	01B4	
SUBTRACTIVE	00	01	00	01B2	INCLUDES LEGACY AND LPC (BIOS)

GPIO USAGE TABLE

DEVICE	NAME	I/O	POWER WELL	DURING RESET	AFTER RESET	USAGE
MCPX	GPIO0	OUT	VCC3	Z	Z	TESTPOINT (NOT USED)
MCPX	GPIO1	OUT	VCC3	H	H	CNFG_SEL1
MCPX	GPIO14	IN	VCC3	Z	Z	CNFG_SEL0
MCPX	GPIO15	OUT	VCC3	Z	Z	TP_DEBUG_GPIO15
MCPX	GPIO16	IN	VCC3	Z	Z	CNFG_SEL2
MCPX	GPIO19	OUT	VCC3	Z	Z	LVLCONT1
MCPX	GPIO20	OUT	VCC3	Z	Z	TESTPOINT (NOT USED)
MCPX	GPIO21	IN	VCC3	H	H	SMI[*] INPUT FROM SMC
MCPX	GPIO22	OUT	VCC3	Z	Z	LVLCONT0
MCPX	GPIO24		VCC3	Z	Z	TESTPOINT (NOT USED)

SMBUS ADDRESS MAP

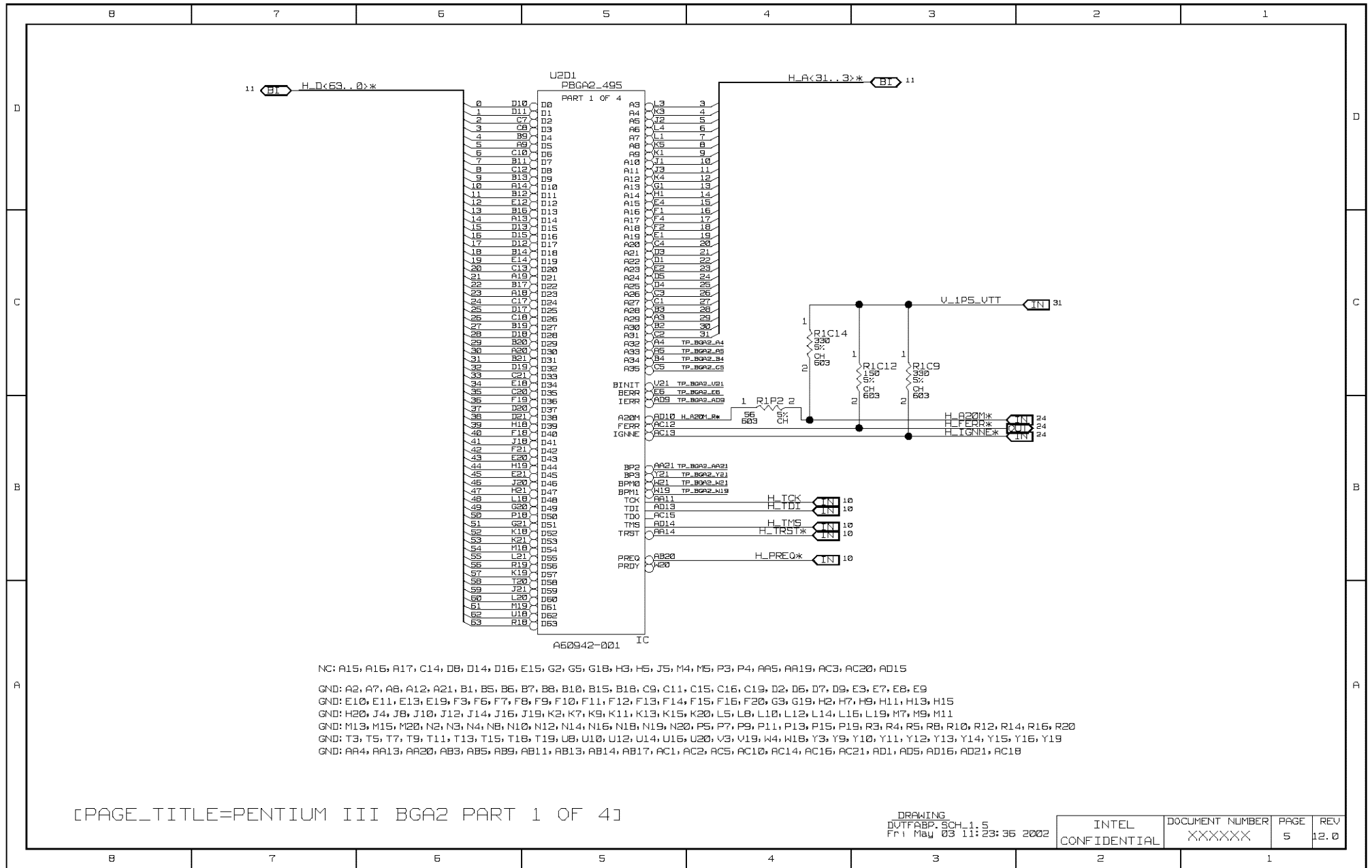
DEVICE	SMBUS #	ADDRESS	EVT	DVT	COMMENTS
CK25871	1	8A/8B		X	CONNECT ALTADDR (PIN 48) TO 3.3
CNR EEPROM	1	A8/A9	X	X	CONNECT CNR_SMB[2:0]=100 BINARY
MCP1 SMB1	1	10/11	X	X	SMBUS HOST (WRITE/READ)
SMC	1	20/21	X	X	(WRITE/READ)
TEMP(ADM1032)	1	98/99	X	X	(WRITE/READ)
DIMM0	0	A0/A1	X		M_A_CS[1..0]*
DIMM1	0	A2/A3	X		M_B_CS[1..0]*
DIMM2	0	A4/A5			M_B_CS[3..2]*
MCP1 SMB0	0	10/11	X		SMBUS HOST (WRITE/READ)

*NOTE: DEVICES ON SMBUS 0 DON'T EXIST ON DVT.

[PAGE_TITLE=GPIO/IDSEL TABLE]

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DVT FAB. SCH. 1.4
Fri May 03 11:23:35 2002

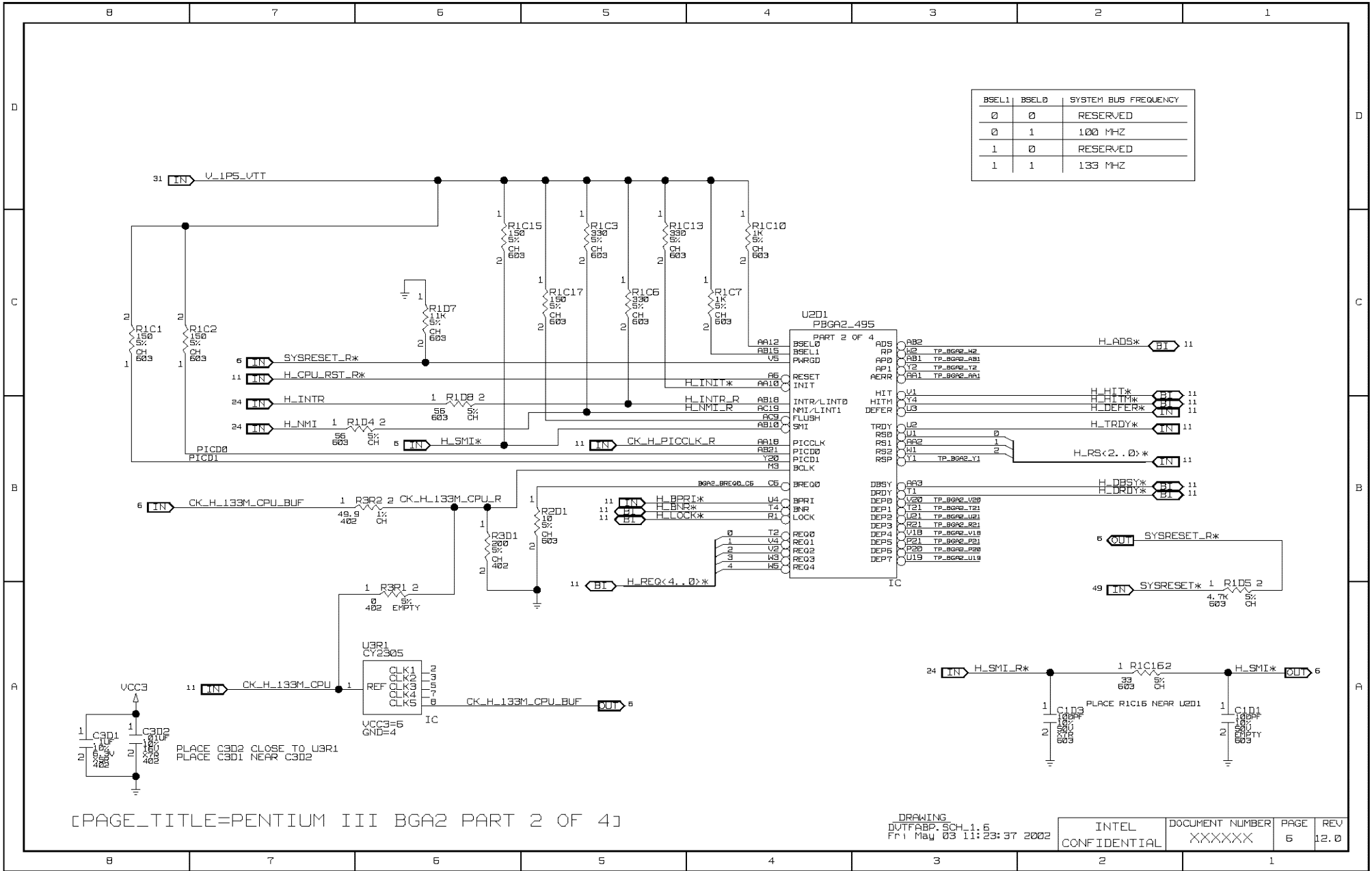
INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 4	REV 12.0
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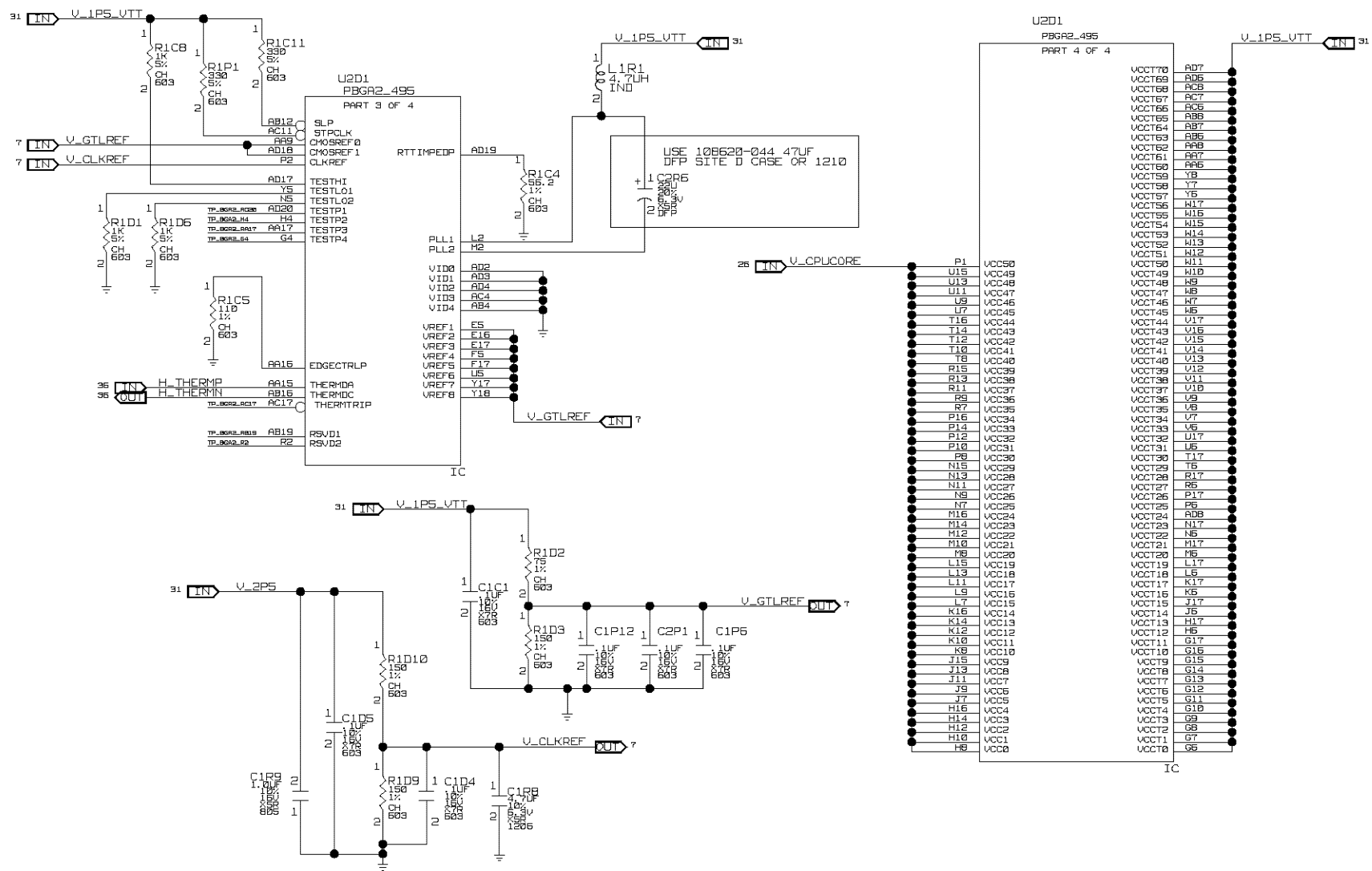


[PAGE_TITLE=PENTIUM III BGA2 PART 1 OF 4]

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DUTFABP_SCH.1.5
Fri May 03 11:23:36 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	5	12.0



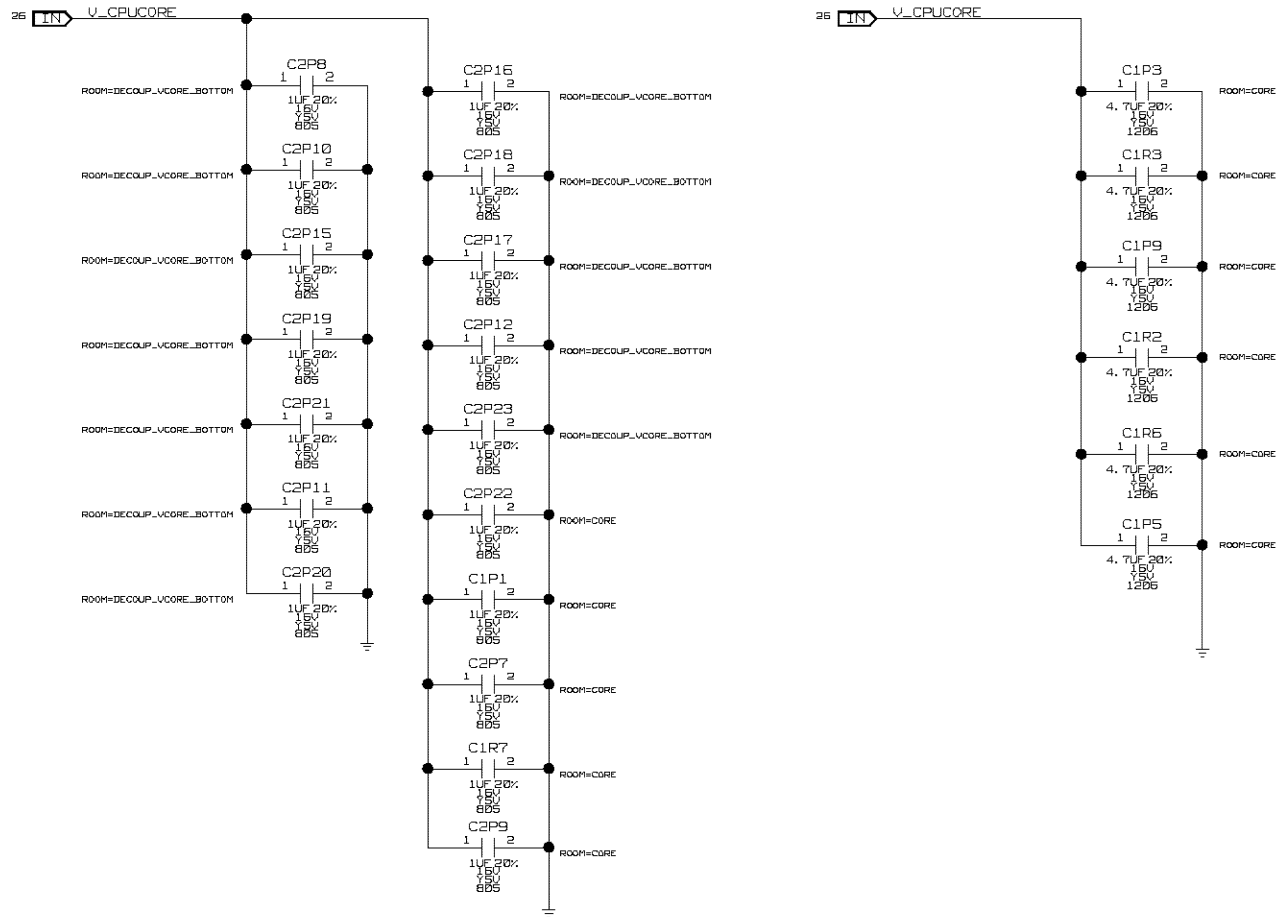


[PAGE_TITLE=PENTIUM III BGA2 PARTS 3 & 4]

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DUT/ABP, SCH 1:7
Fri May 03 11:23:37 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	7	12.0

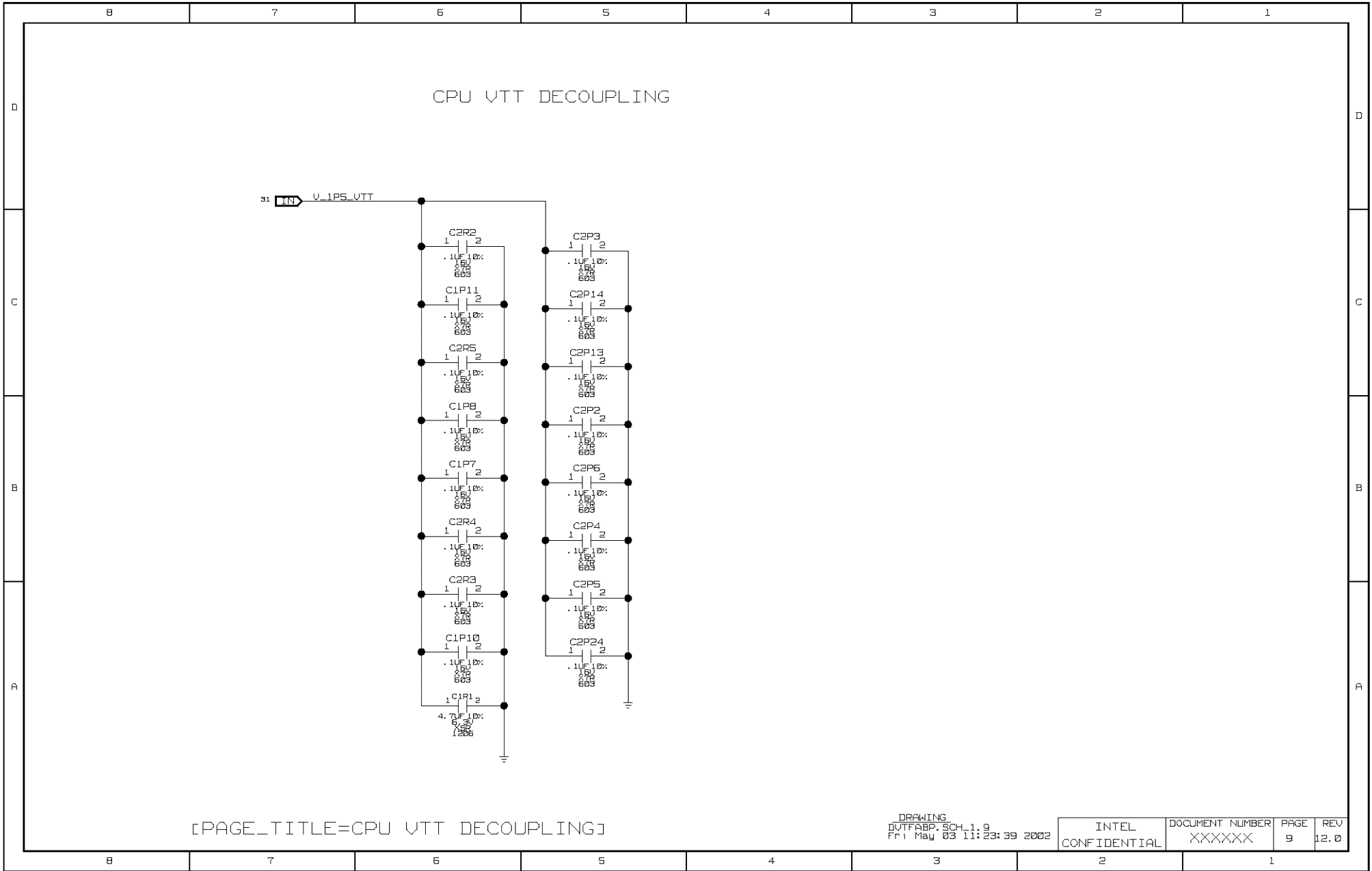
CPU VCORE DECOUPLING

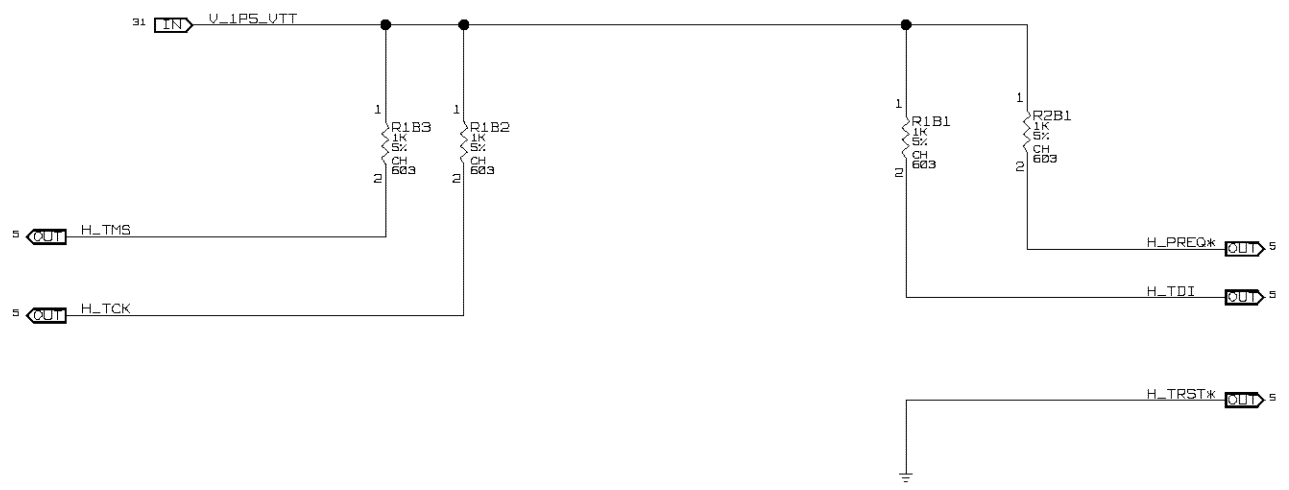


[PAGE_TITLE=CPU VCORE DECOUPLING]

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OUTFABP. SCH. 1.8
Fri May 03 11:23:38 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 8	REV 12.0
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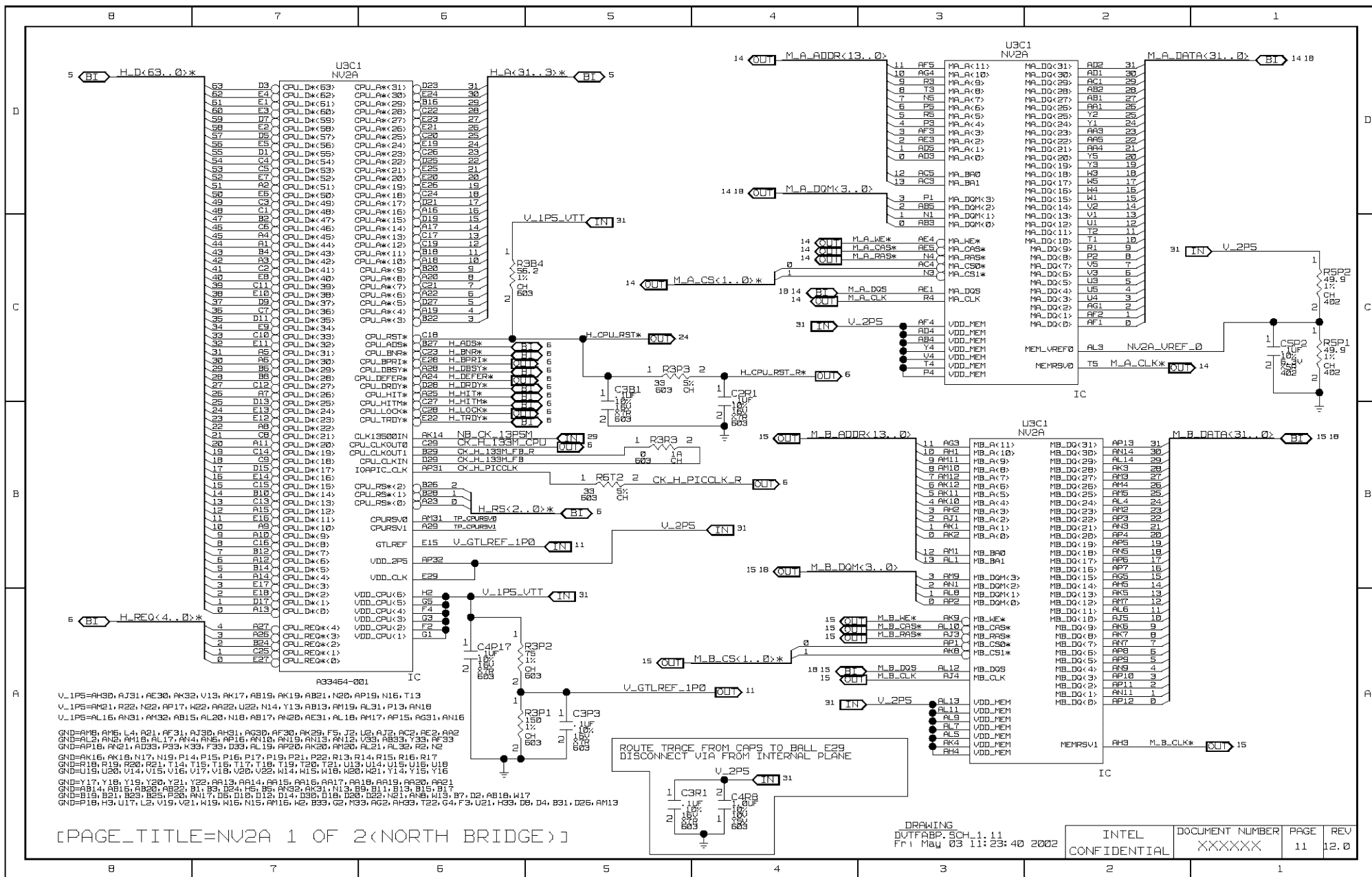


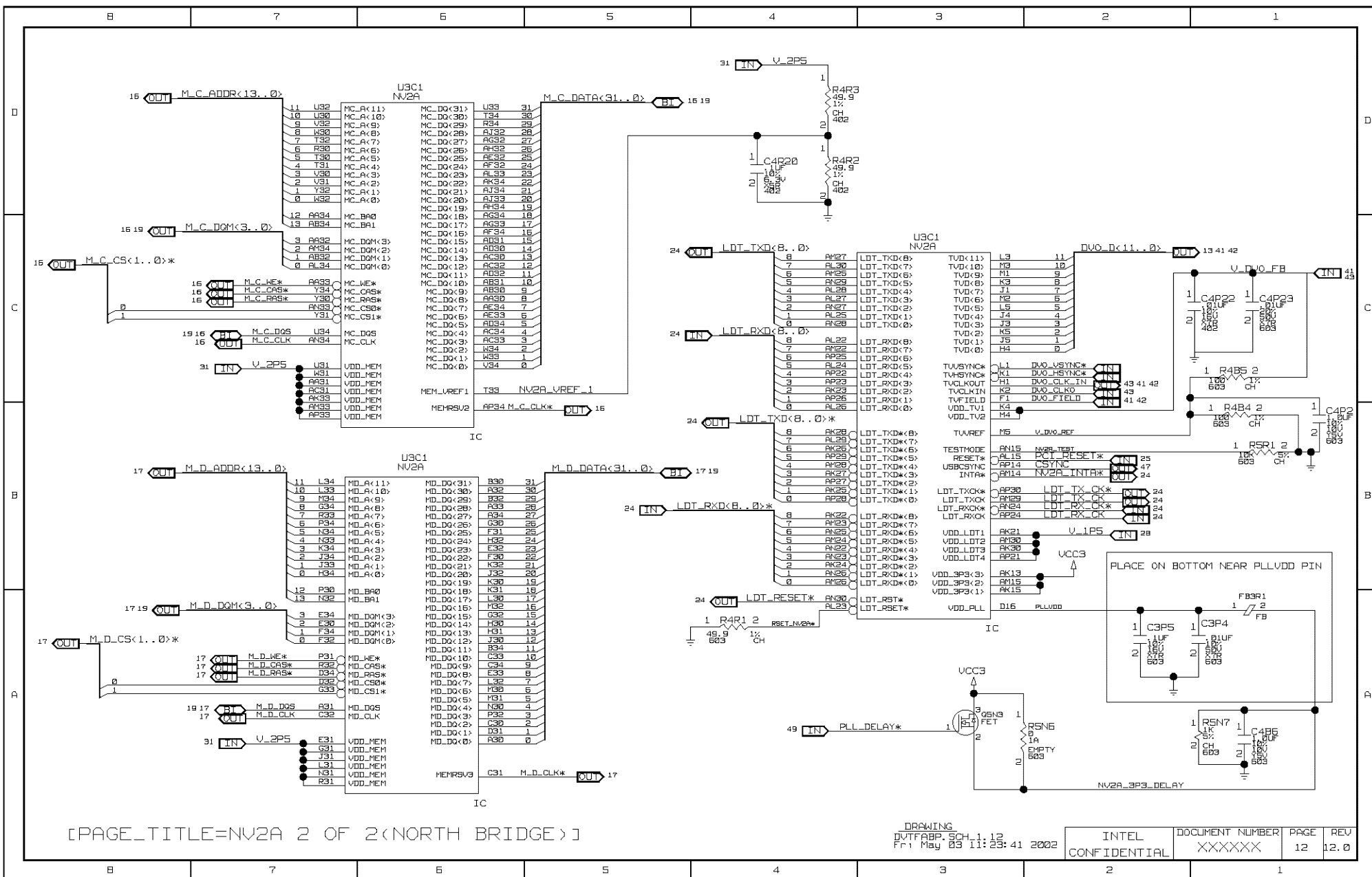


[PAGE_TITLE=ITP TERMINATION]

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DUTFABP.SCH.1.10
Fri May 03 11:23:39 2002

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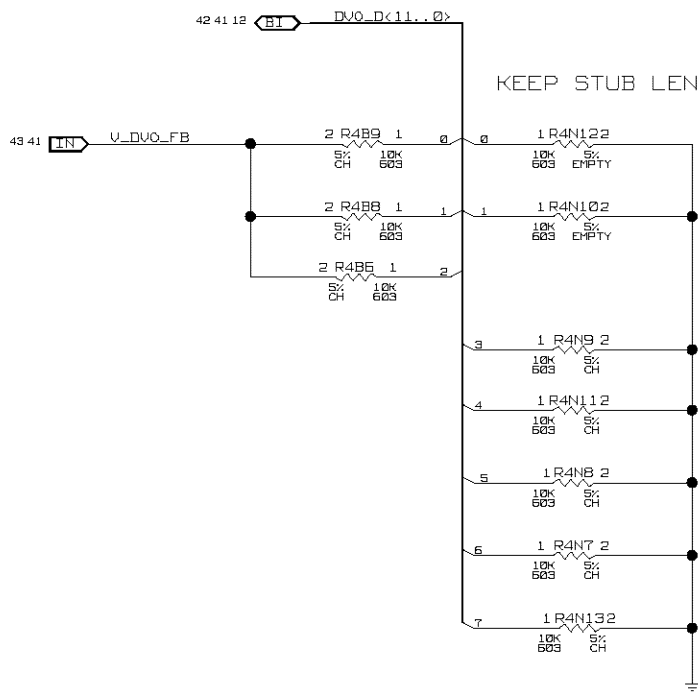
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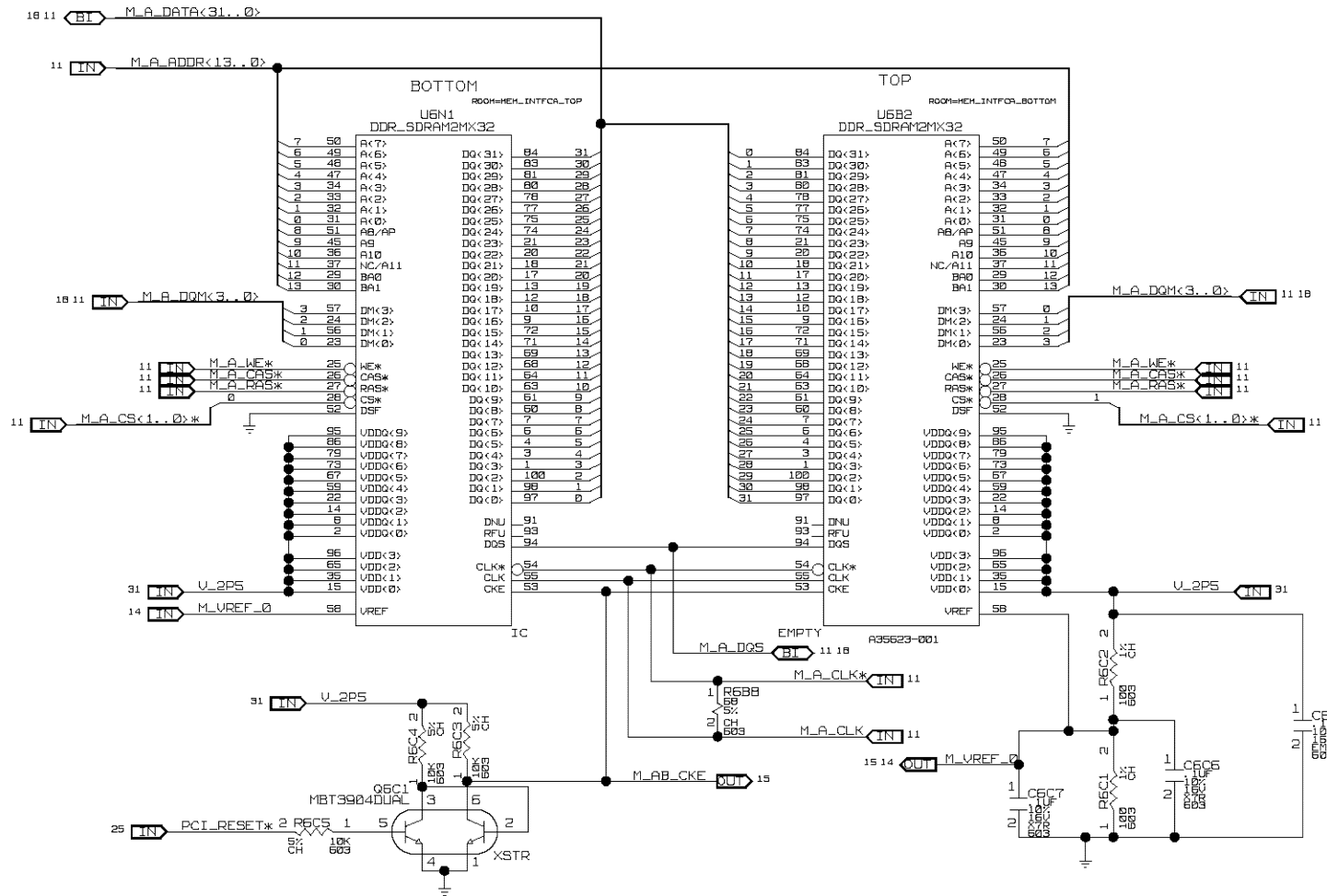


TV[D		DEFINITION
[7]	0* 1	ENABLE INTERNAL LDT TERMINATION DISABLE INTERNAL LDT TERMINATION
[6]	0* 1	13.5MHZ OR 16.6MHZ 14.31818MHZ
[5:4]	00* 01 10 11	USE FSB FREQUENCY BASED ON TVD[3:2] USE INTERNAL PROGRAMMED VALUE A USE INTERNAL PROGRAMMED VALUE B FORCE 55MHZ
[3:2]	00 01* 10 11	NA FSB FREQ=133MHZ FOR 16.6MHZ INPUT CLK NA NA
[1:0]	00* 01 10 11	EMRS MICRON MATCHED MODE EMRS [6,11]=[0,1], HALF OF NORMAL DRIVE MODE RESERVED EMRS MATCHED 30% DRIVE MODE<SAMSUNG>

* = CURRENT SETTING

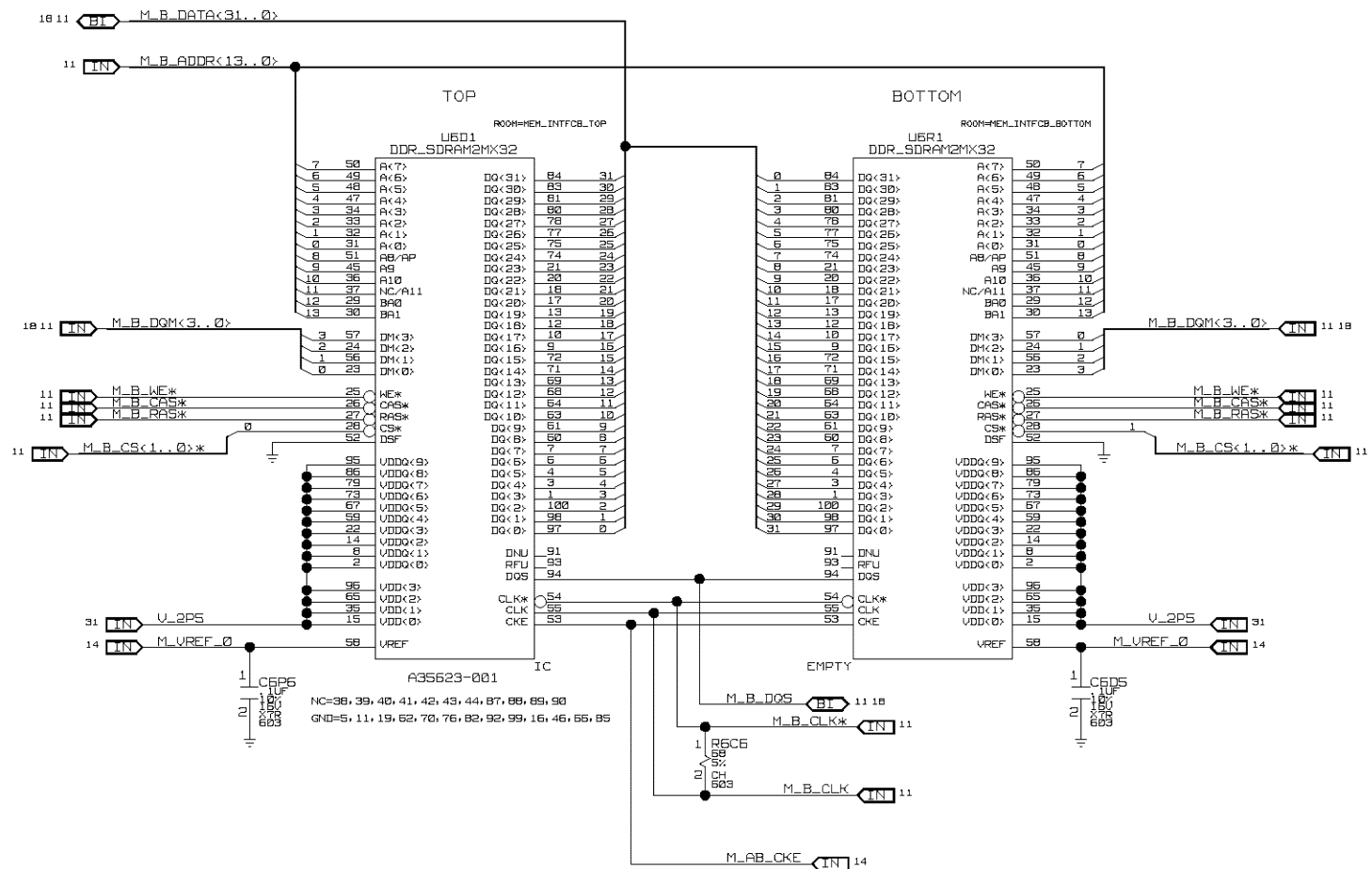
FOR SAMSUNG DDR:
EMPTY R4N10 AND R4N12
STUFF R4B8 AND R4B9

MEMORY INTERFACE PARTITION A

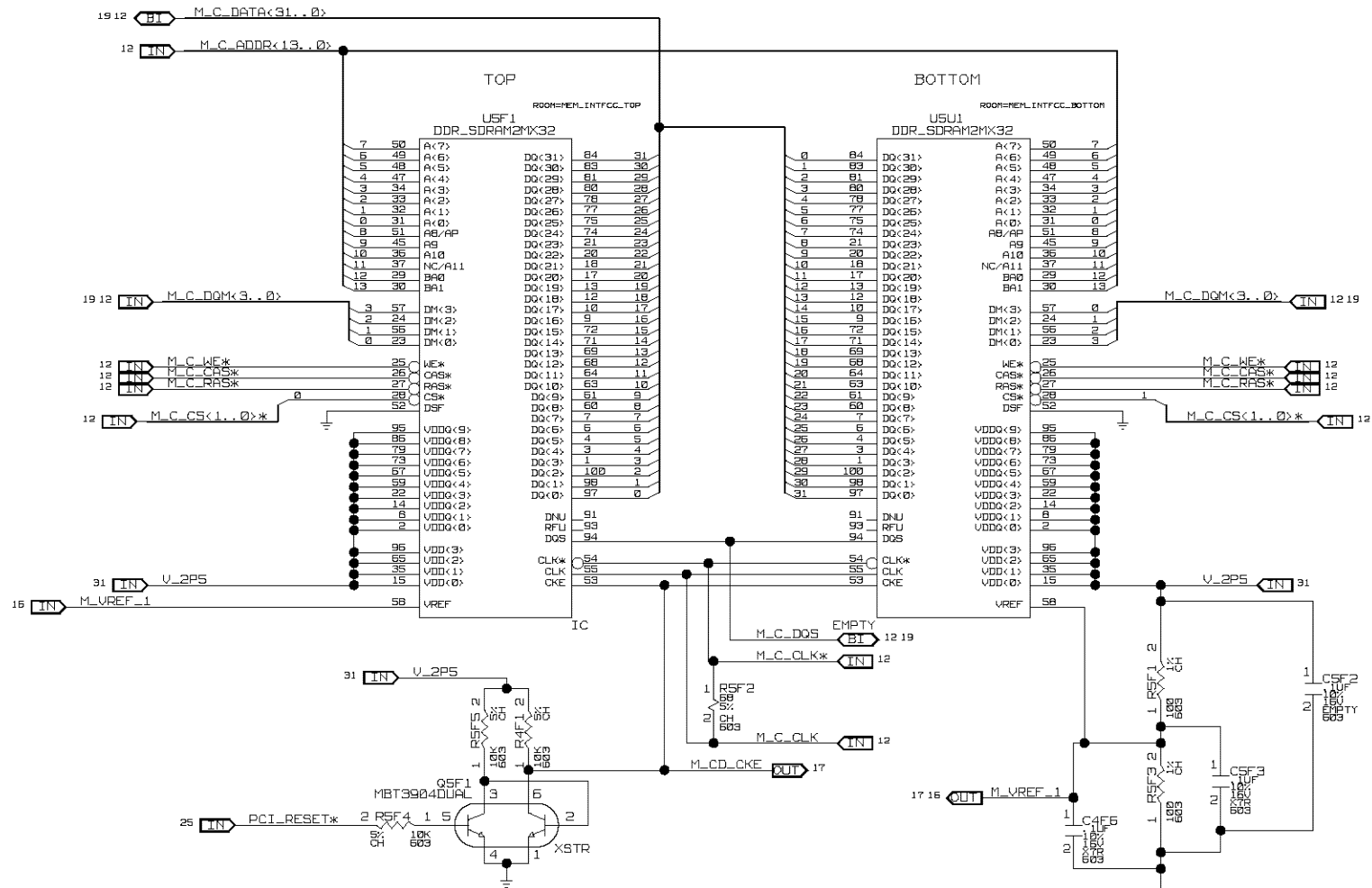


[PAGE_TITLE=DDR SDRAM (PARTITION A)]

MEMORY INTERFACE PARTITION B



MEMORY INTERFACE PARTITION C

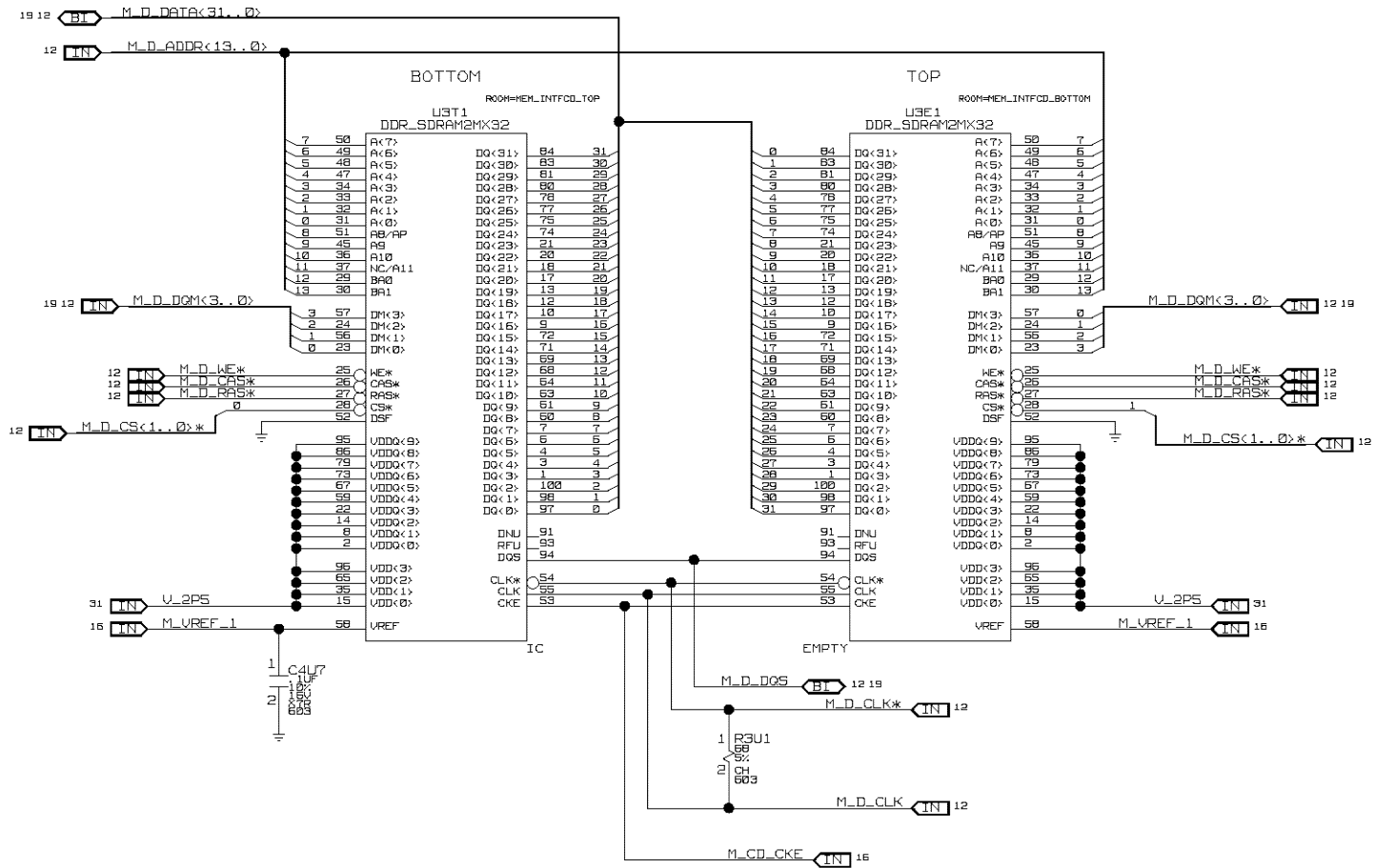


[PAGE_TITLE=DDR SDRAM (PARTITION C)]

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OUTFABP_SCH.1:16
Fri May 03 11:23:44 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 16	REV 12.0
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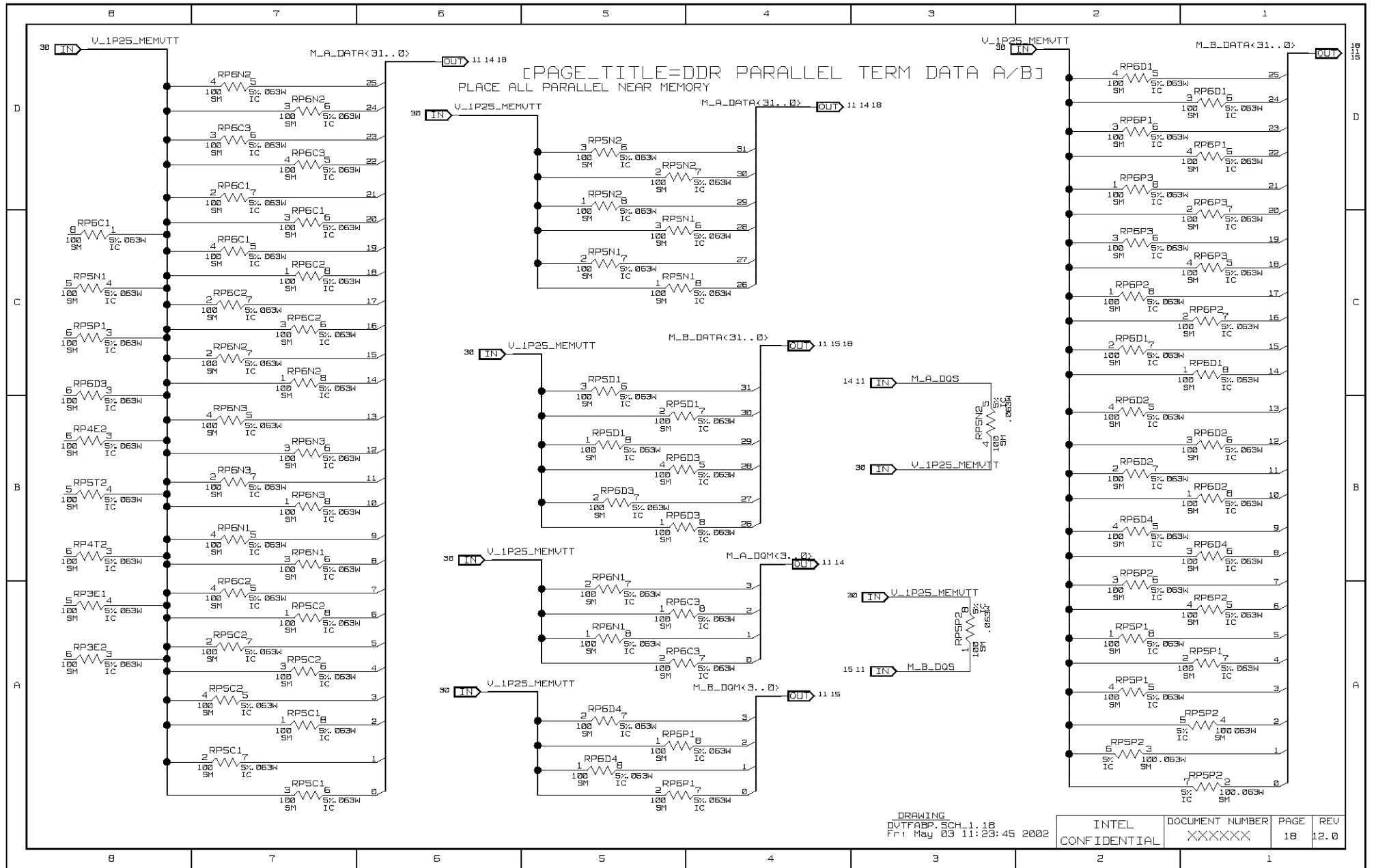
MEMORY INTERFACE PARTITION D



[PAGE_TITLE=DDR SDRAM (PARTITION D)]

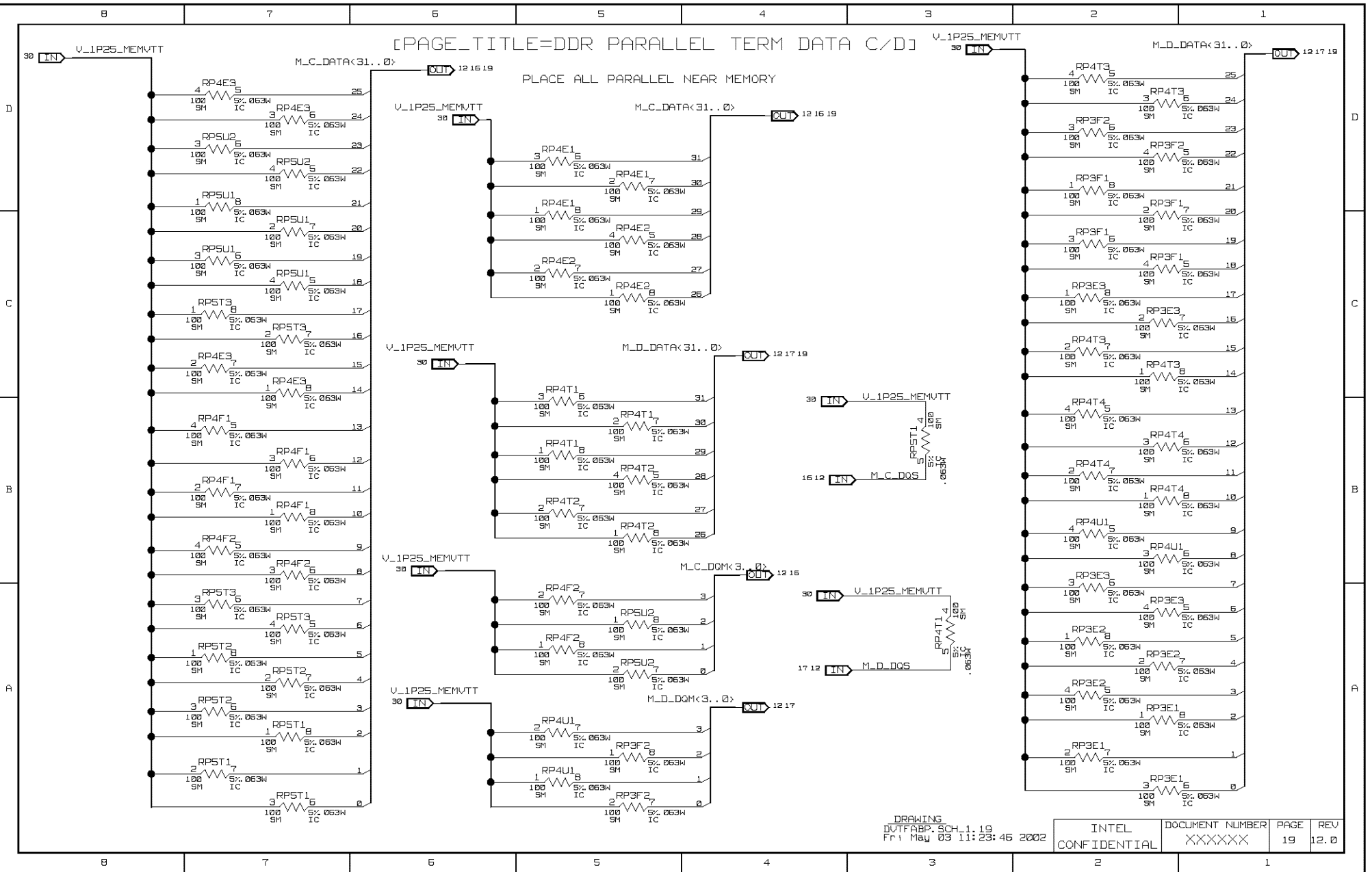
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OUTFABP_SCH.1.17
Fri May 03 11:23:45 2002

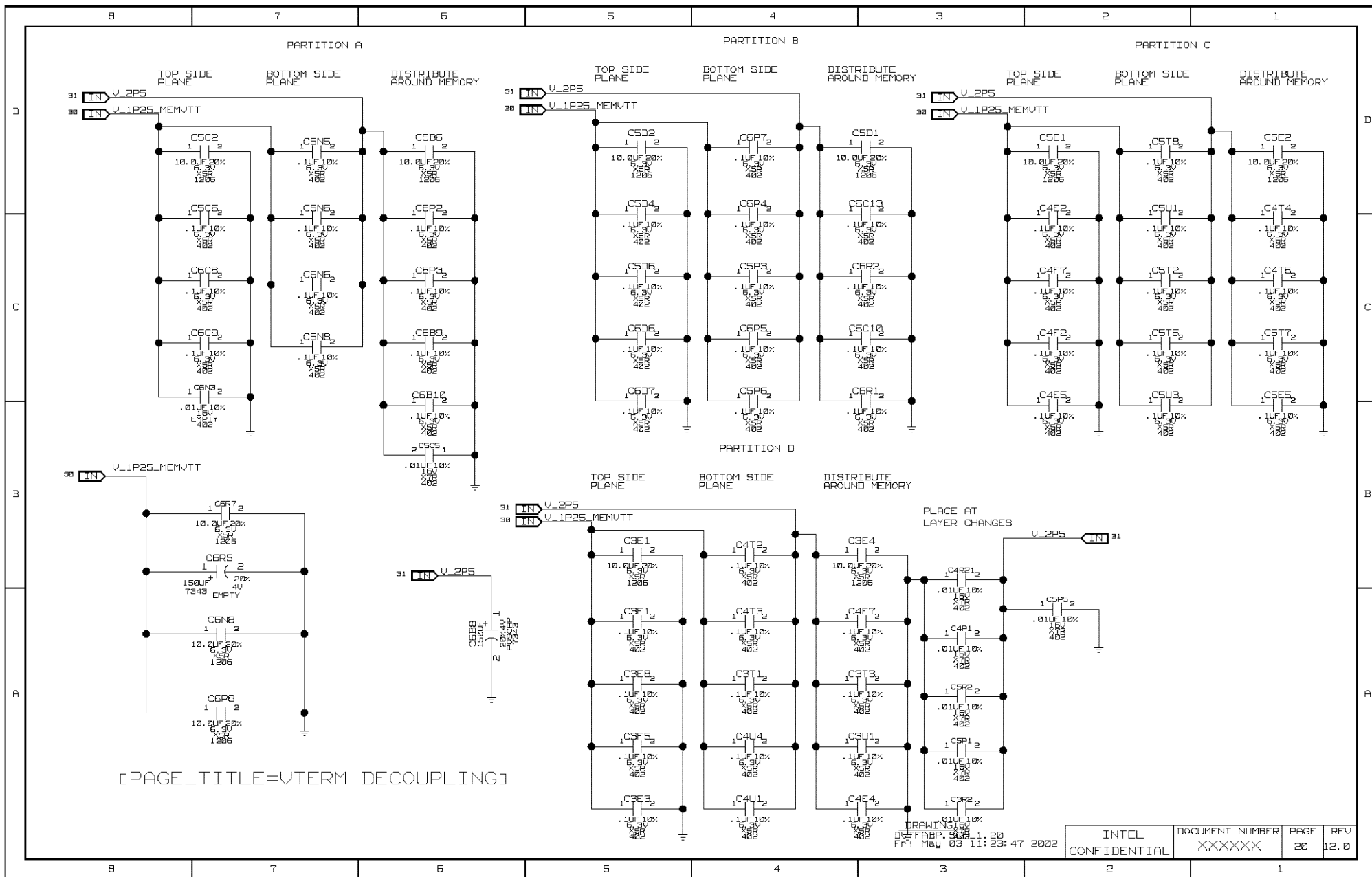
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	17	12.0



[PAGE_TITLE=DDR PARALLEL TERM DATA C/D]

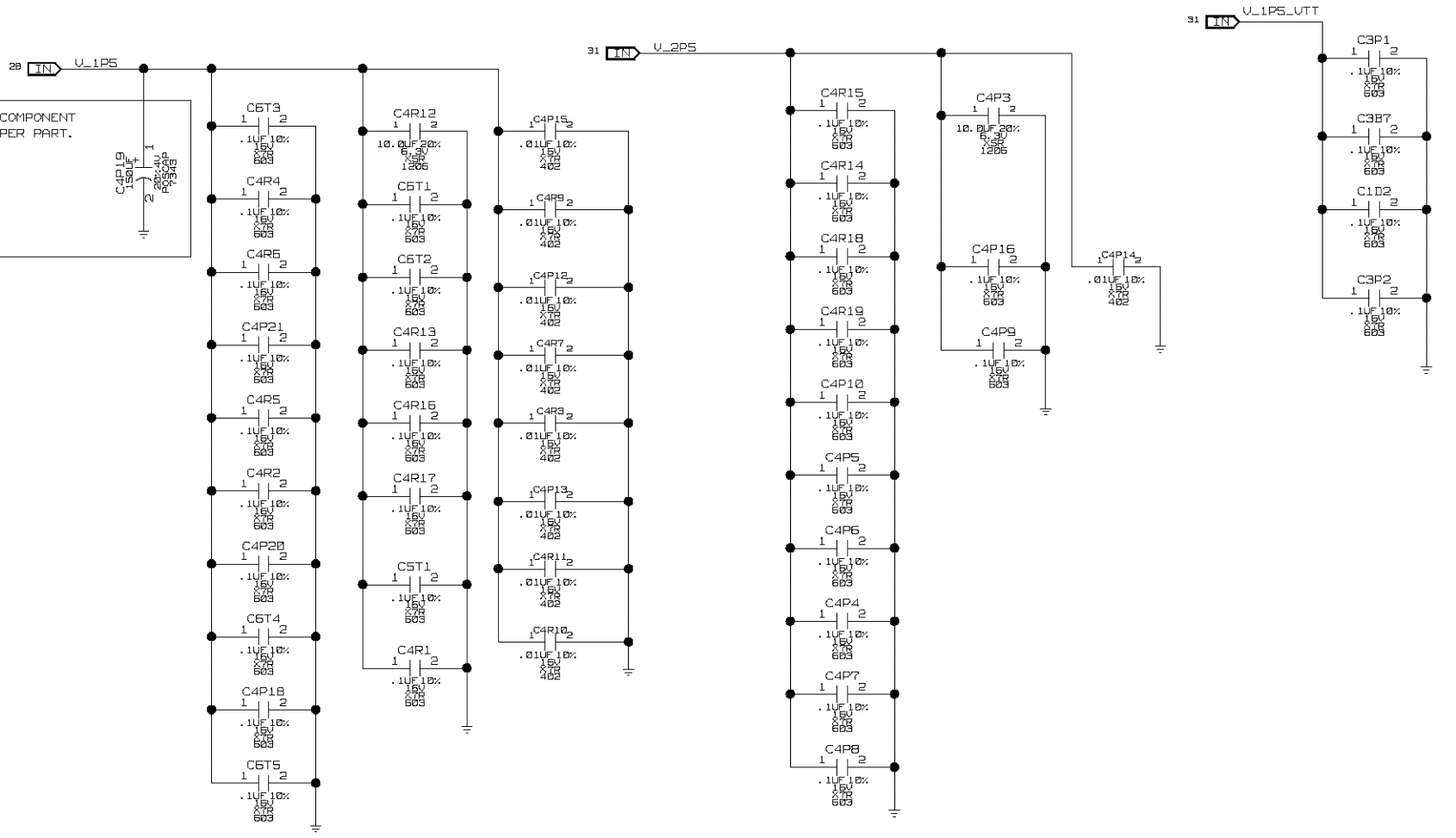
PLACE ALL PARALLEL NEAR MEMORY





NV2A DECOUPLING

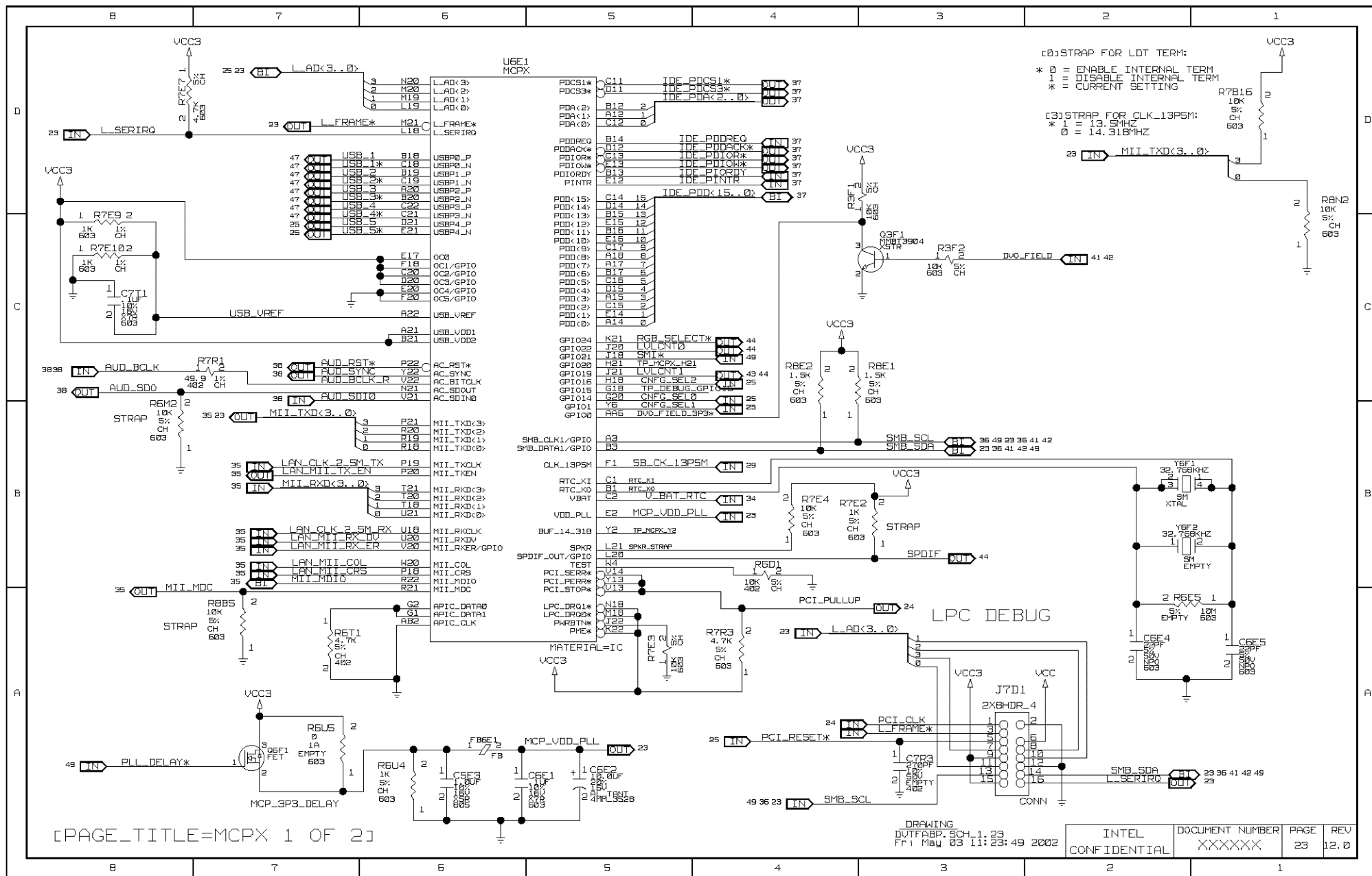
CHANGE COMPONENT
TO CHEAPER PART.

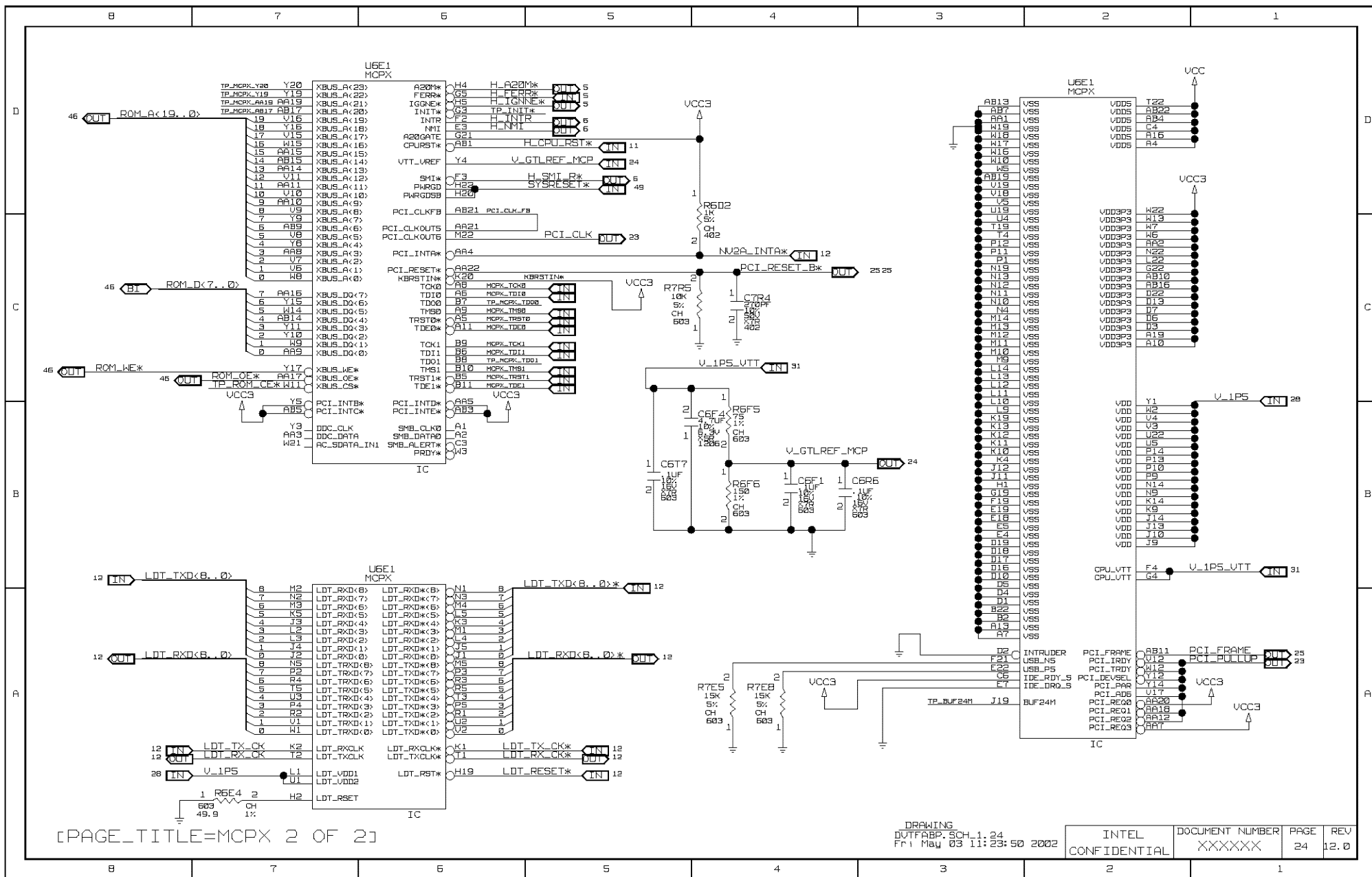


[PAGE_TITLE=NV2A DECOUPLING]

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DUTFABP. SCH. 1:22
Fri May 03 11:23:49 2002

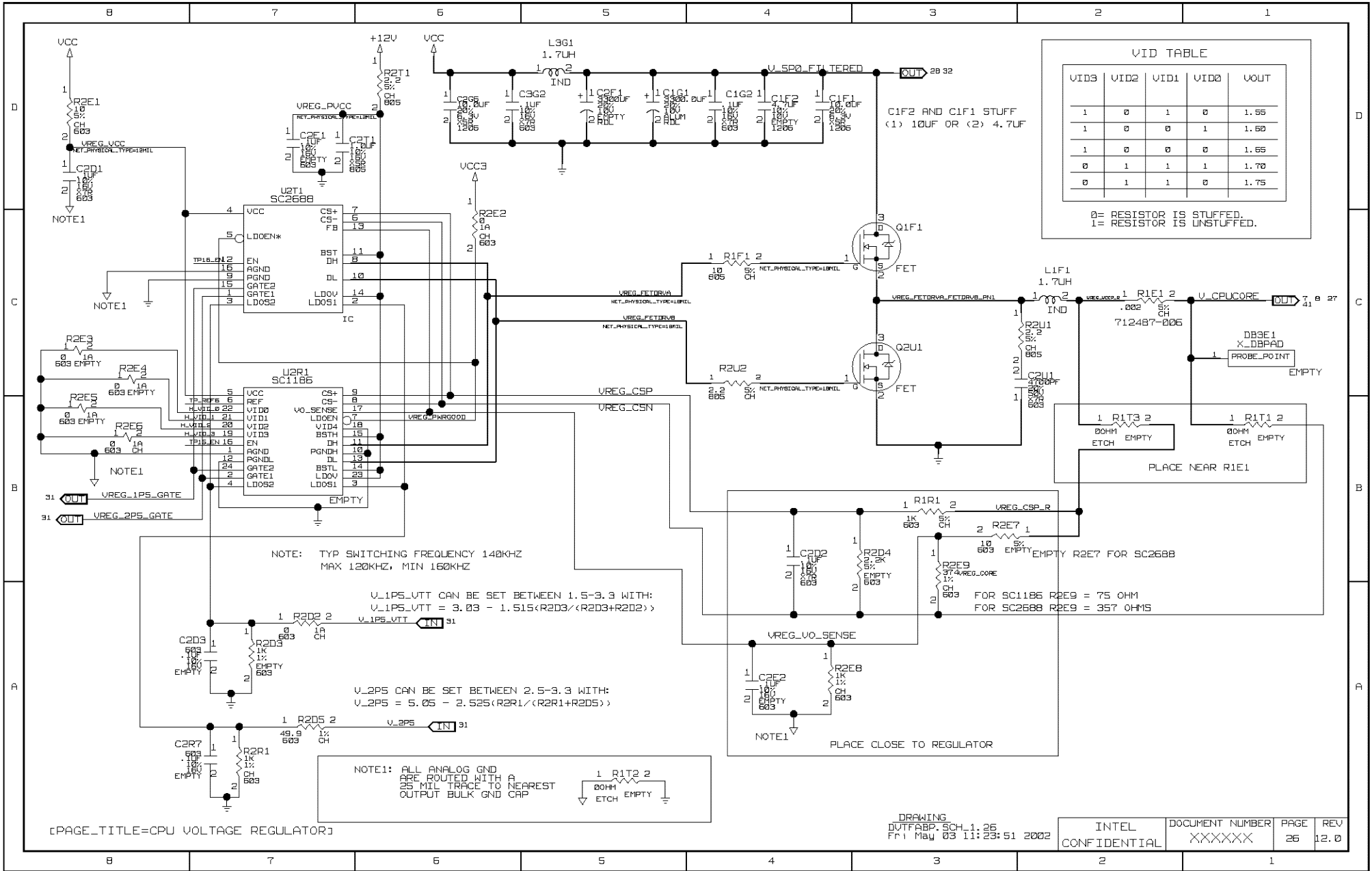
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	22	12.0

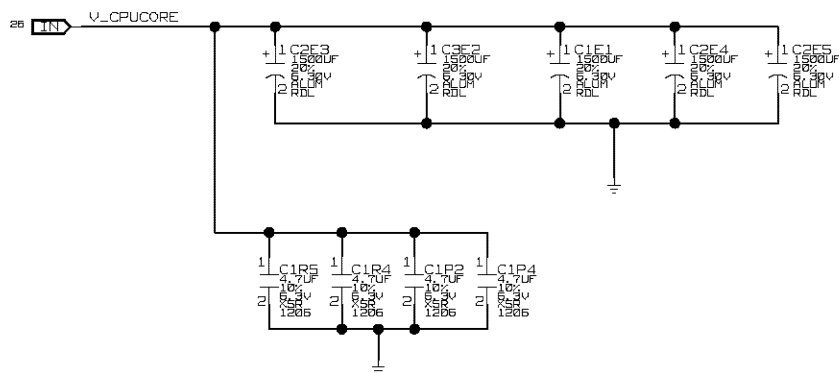




* = CURRENT SETTING



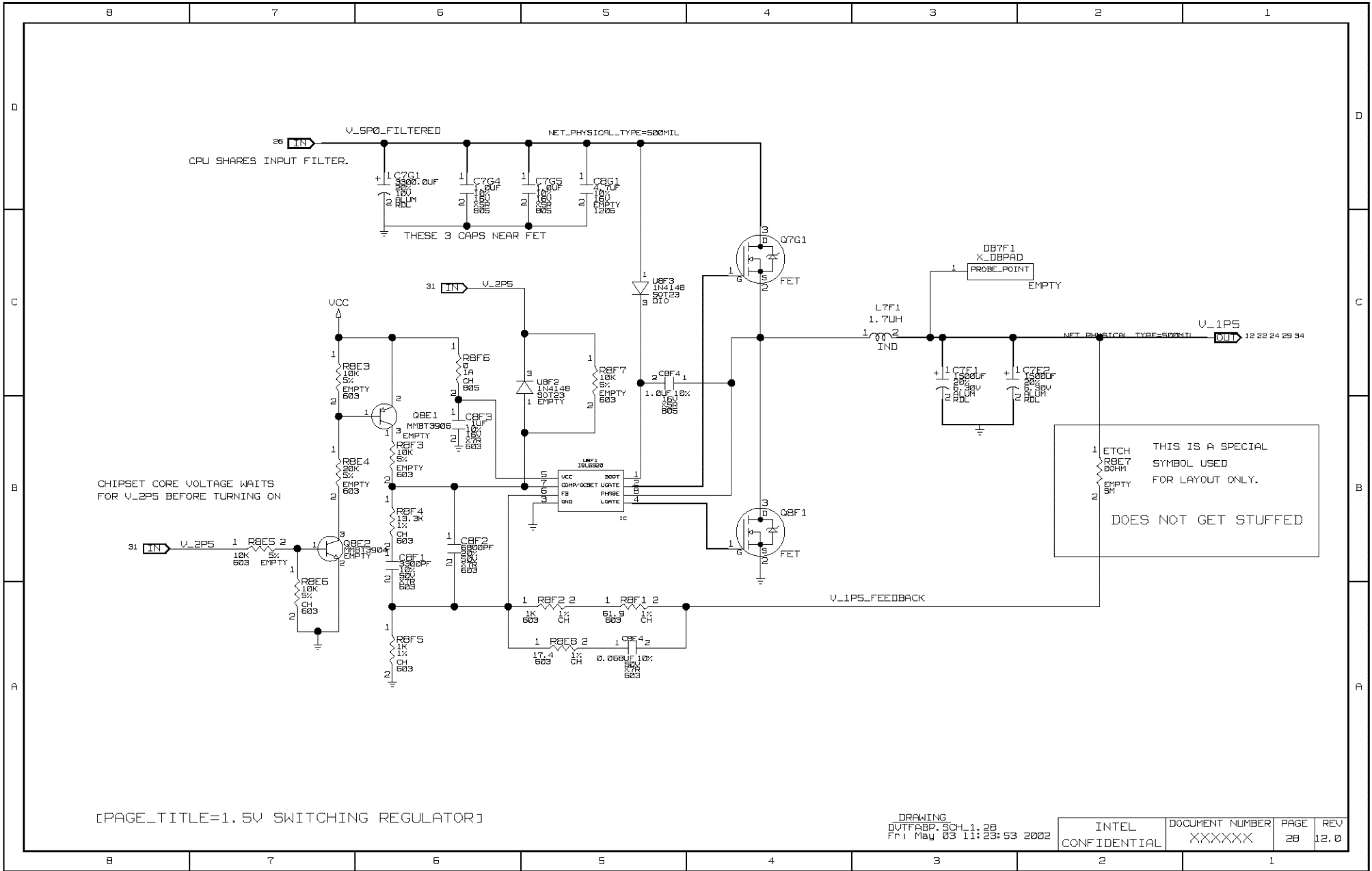


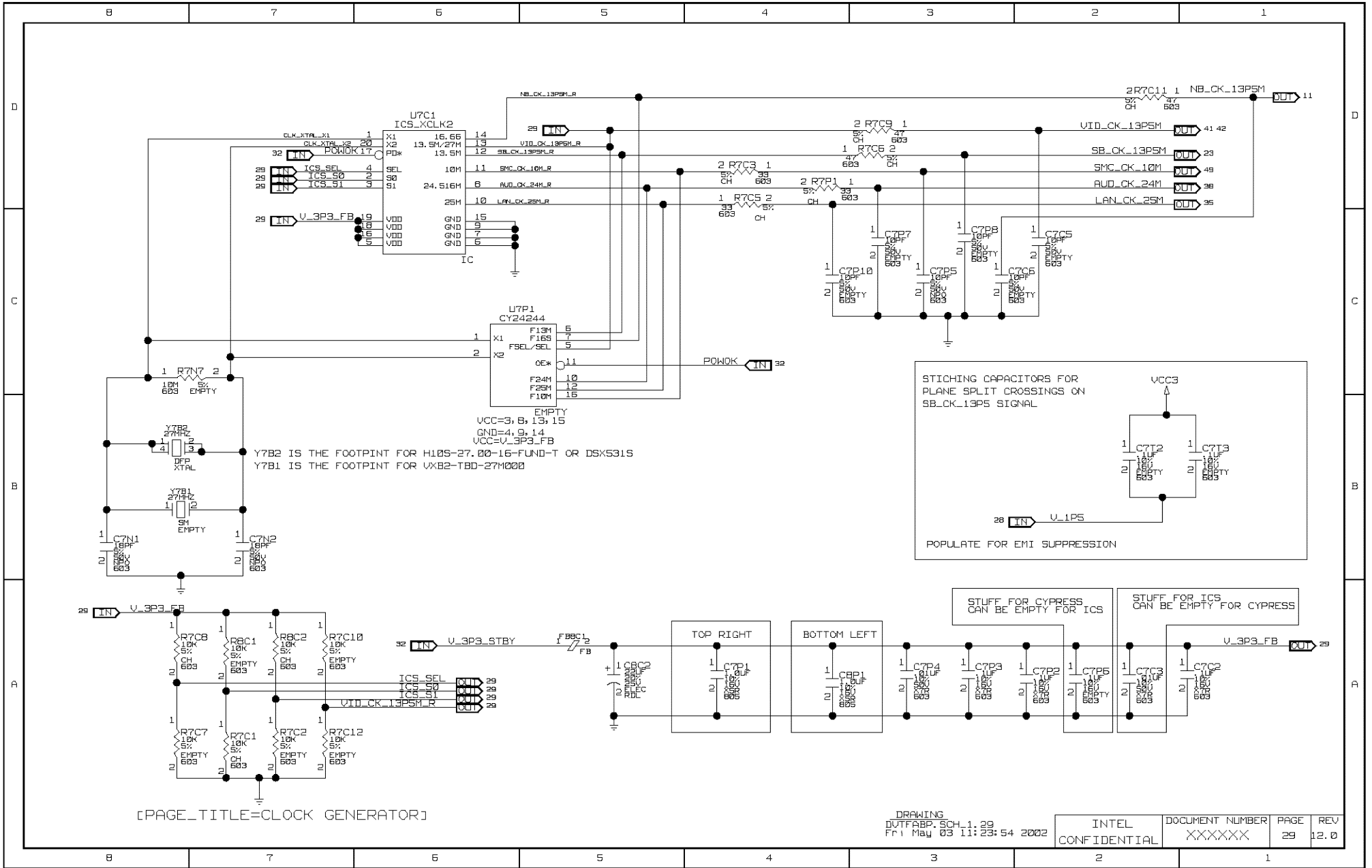


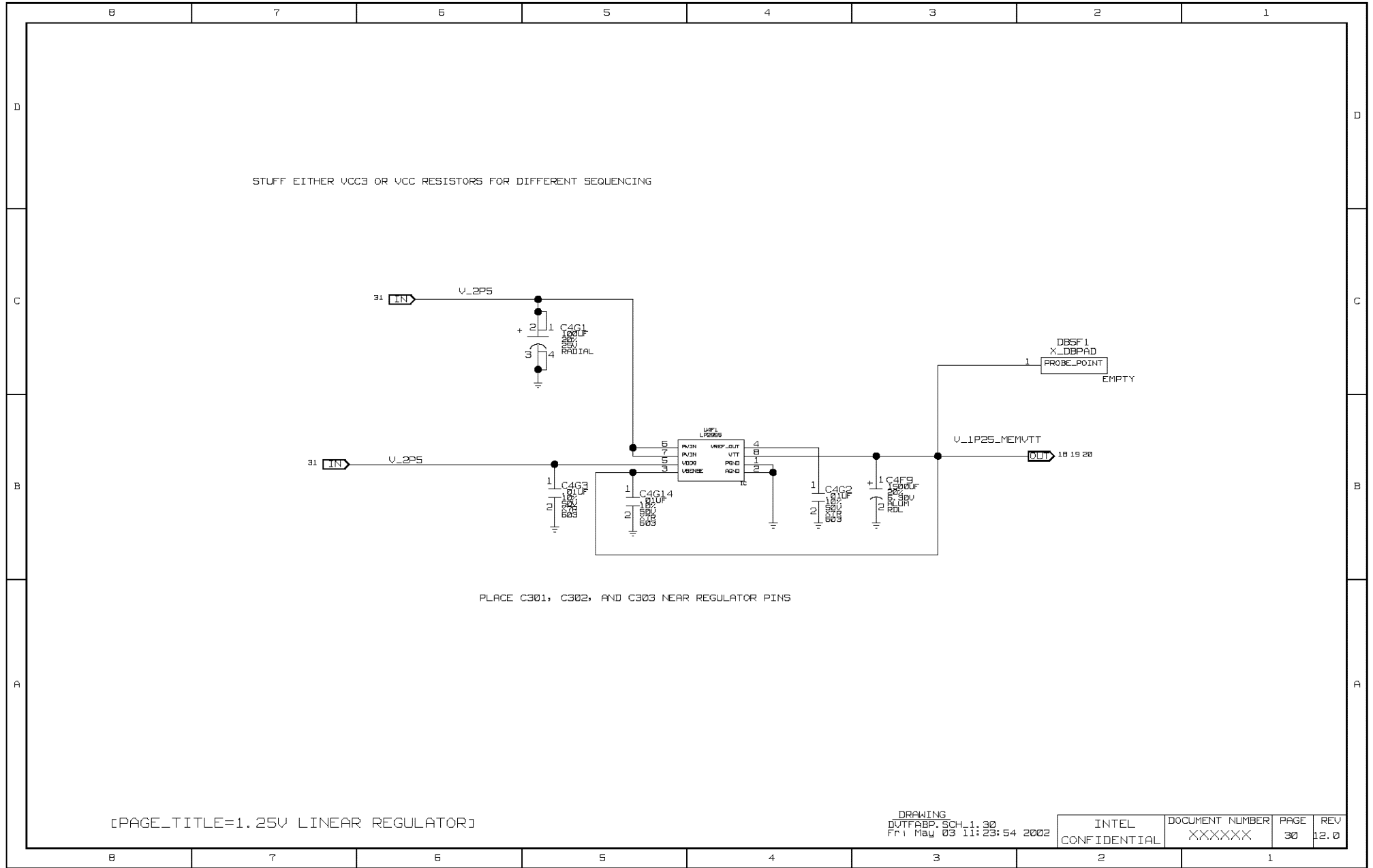
[PAGE_TITLE=CPU VREG OUTPUT FILTER]

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Fri May 03 11:23:52 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 27	REV 12.0
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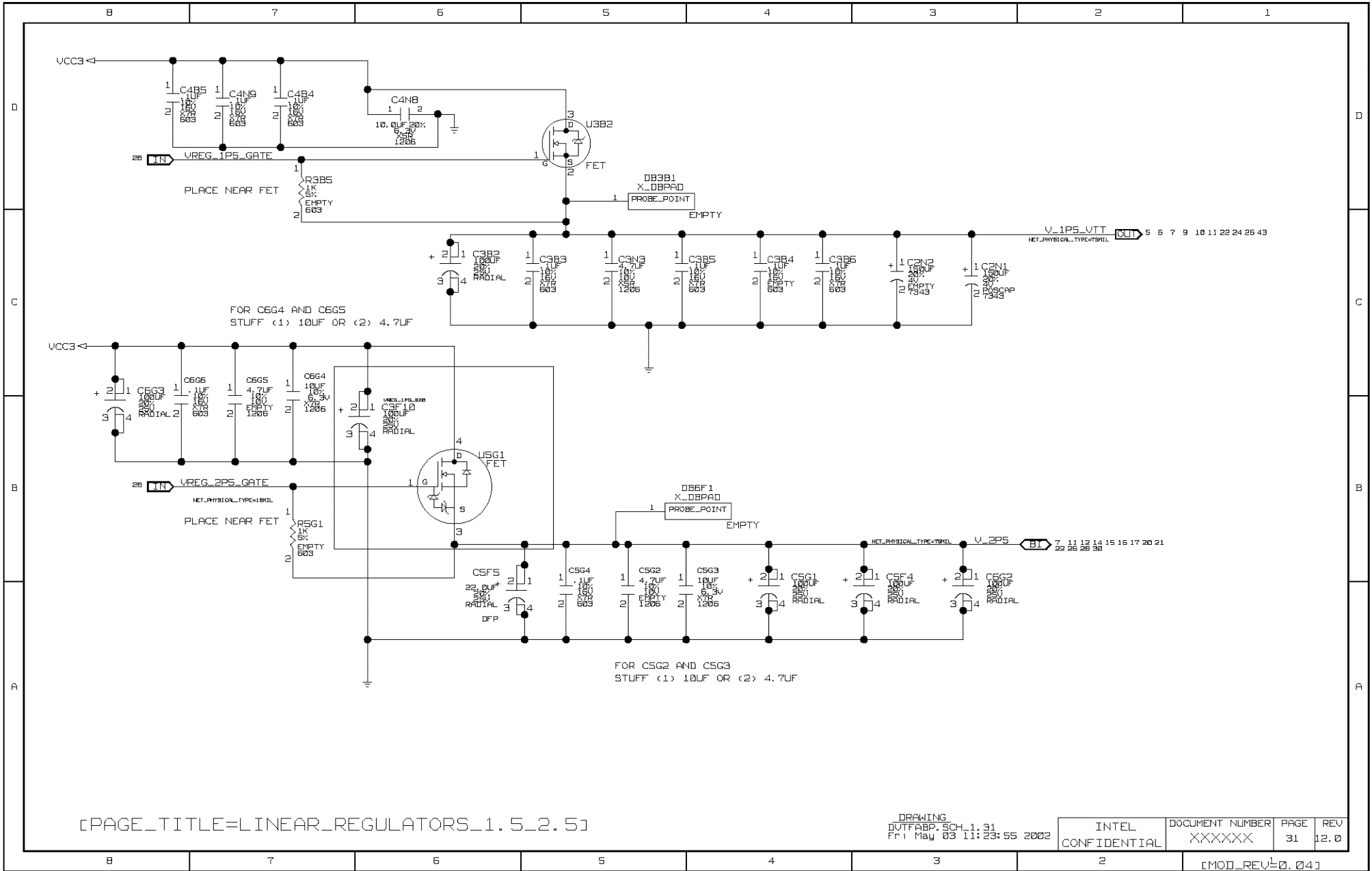


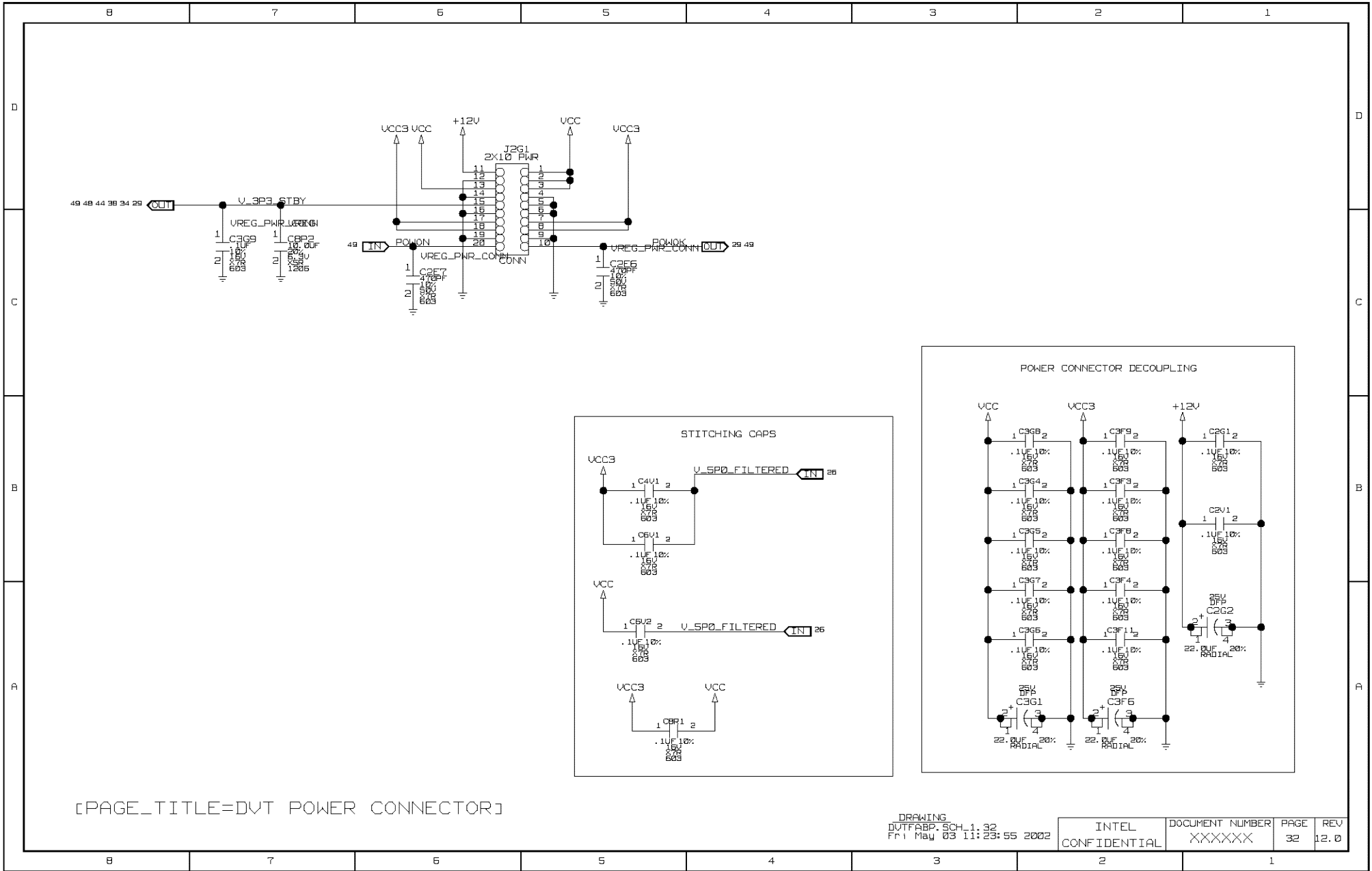




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OUTFABP.SCH.1:30
Fri May 03 11:29:54 2002

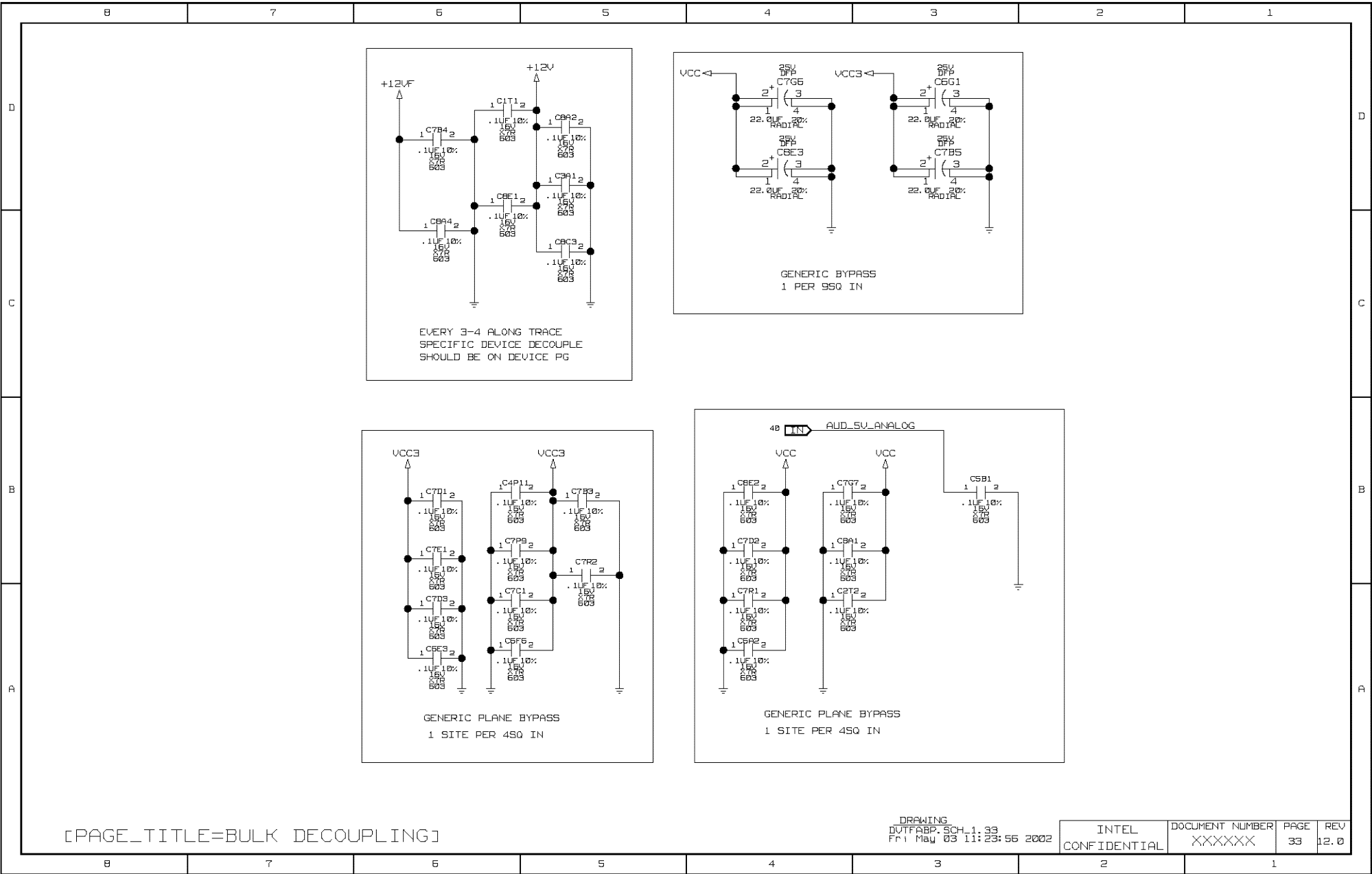
INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 30	REV 12.0
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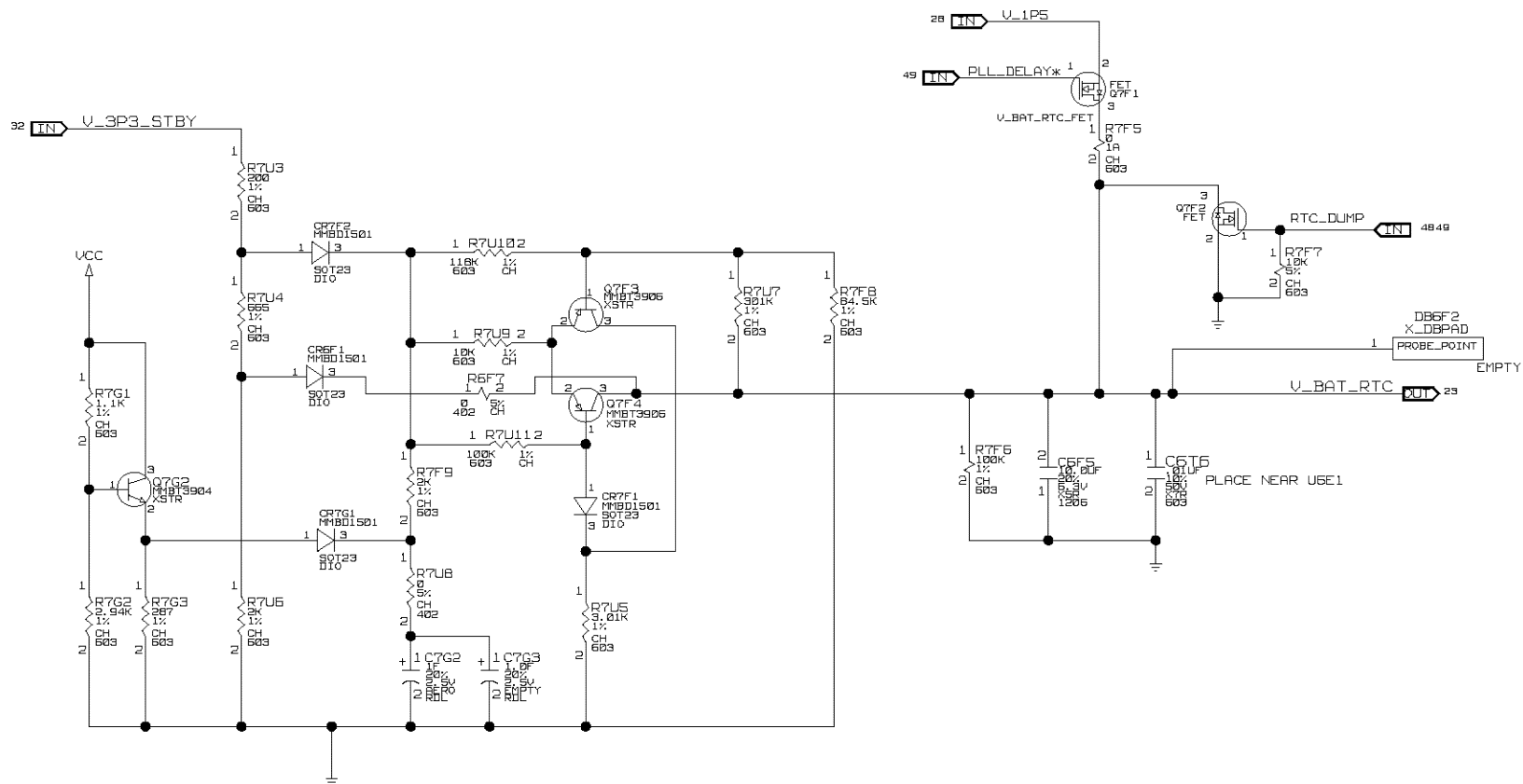




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DVT FASP, SCH. 1: 32
Fri May 03 11:29:55 2002

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CONFIDENTIAL	XXXXXX	32	12.0

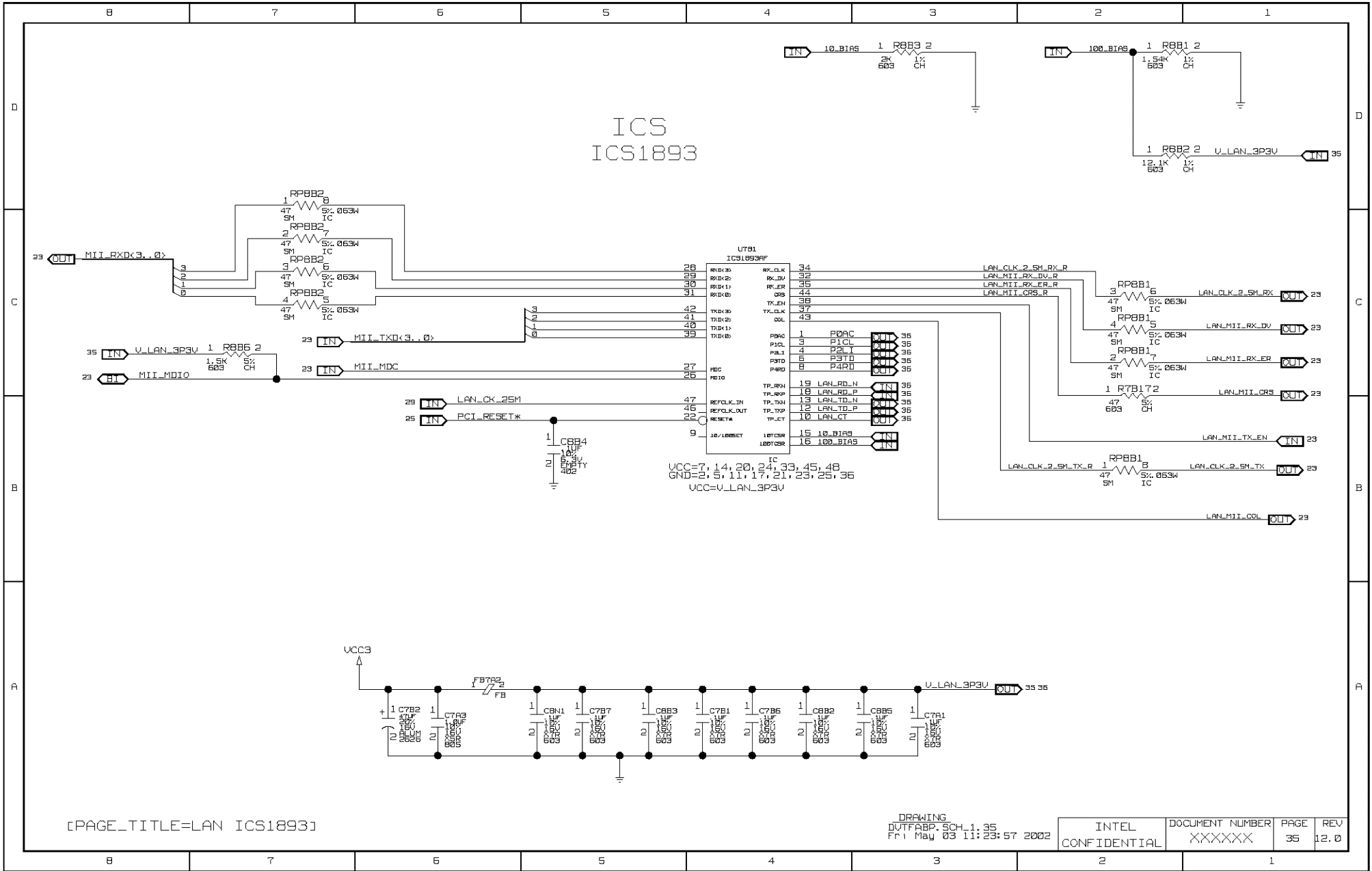




[PAGE_TITLE=SUPERCAP VBAT REGULATOR]

DRAWING
DUTFABP_SCH.1_34
Fri May 03 11:23:57 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 34	REV 12.0
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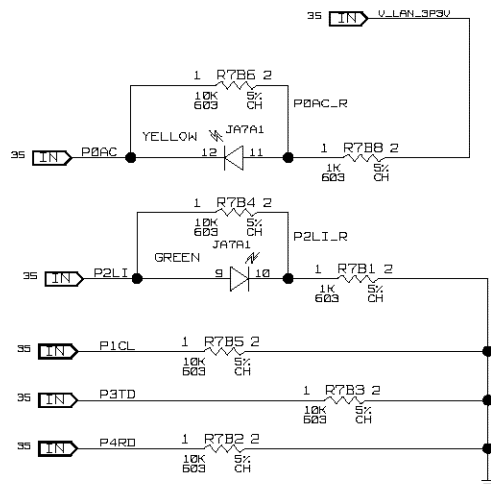
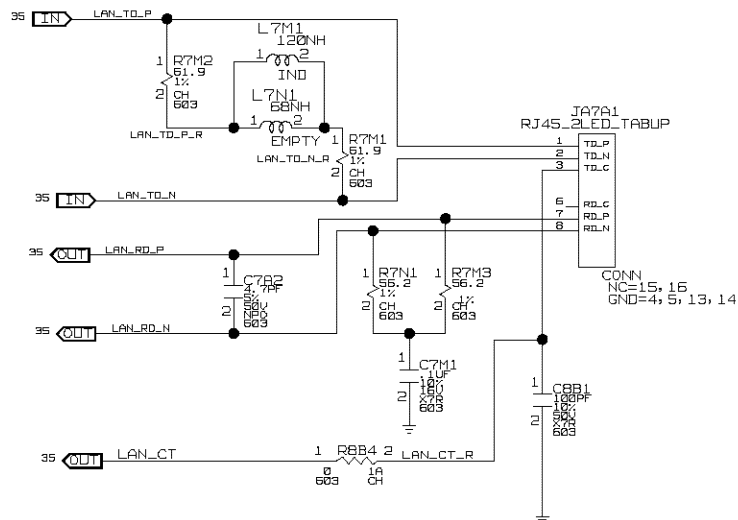


[PAGE_TITLE=LAN ICS1893]

DRAWING
OUTFABP. SCH. 1: 35
Fri May 03 11:23:57 2002

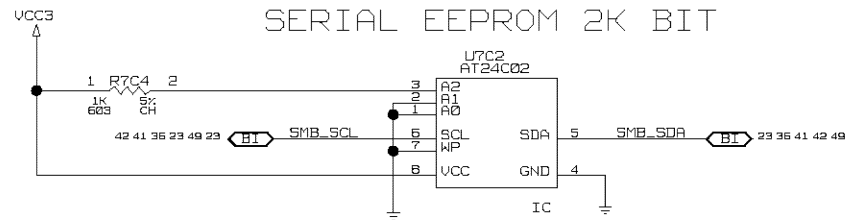
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	35	12.0

RJ45 SP JACK

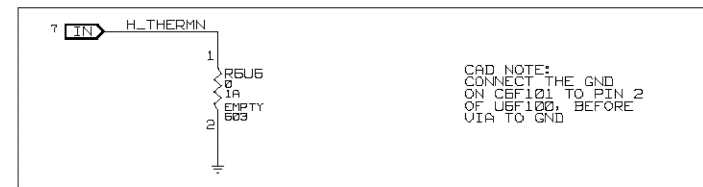
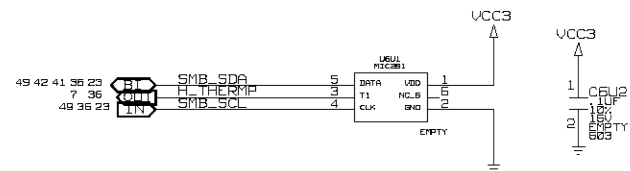
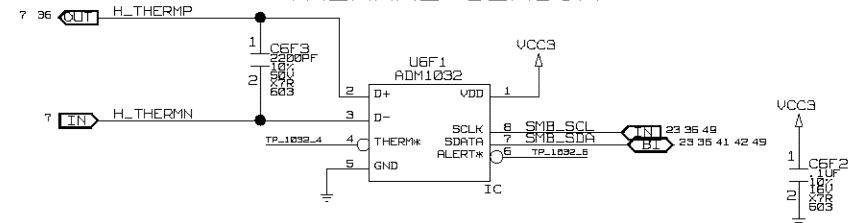


[PAGE_TITLE=LAN JACK/THERMAL SENSE/EEPROM]

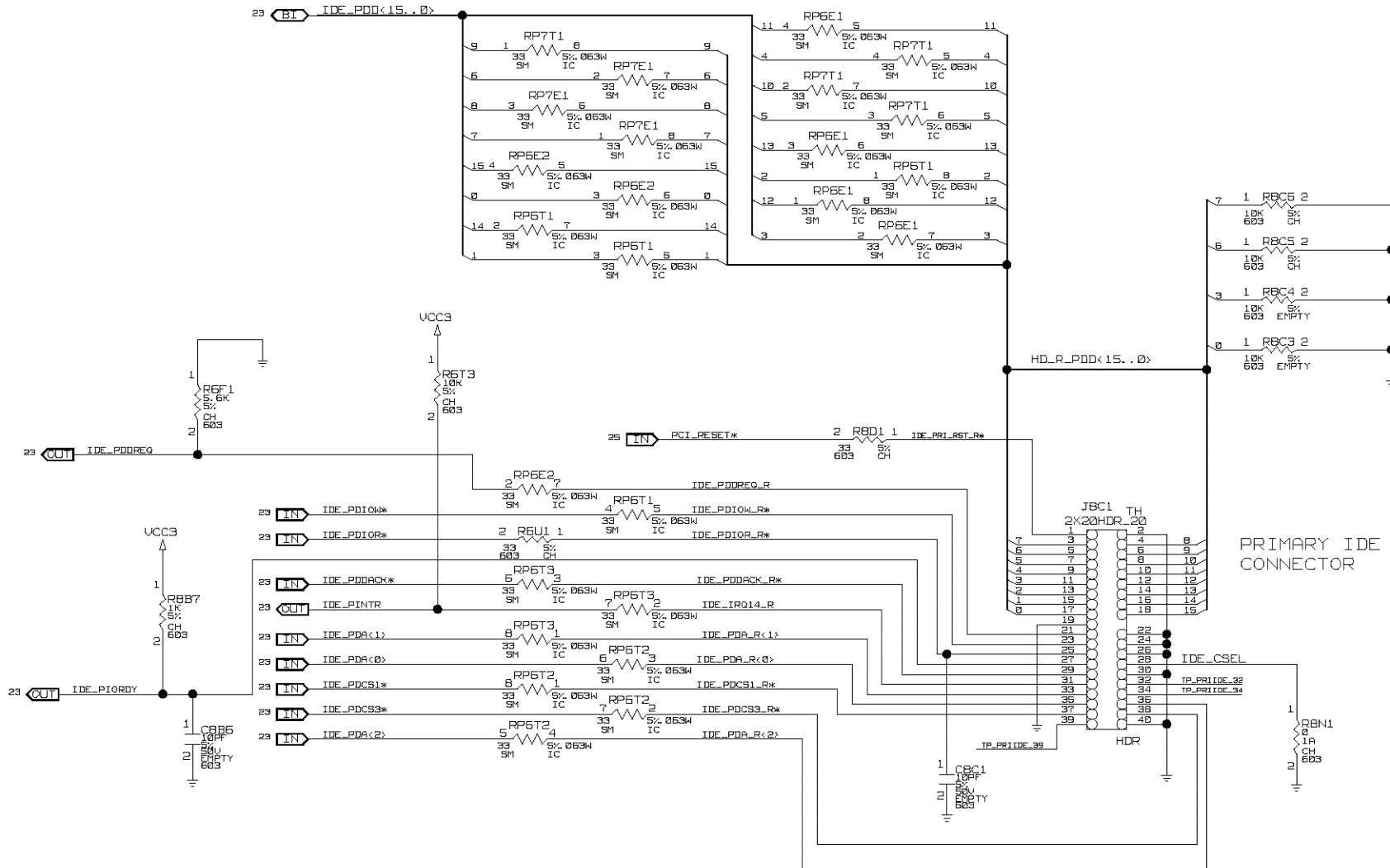
SERIAL EEPROM 2K BIT



THERMAL SENSOR



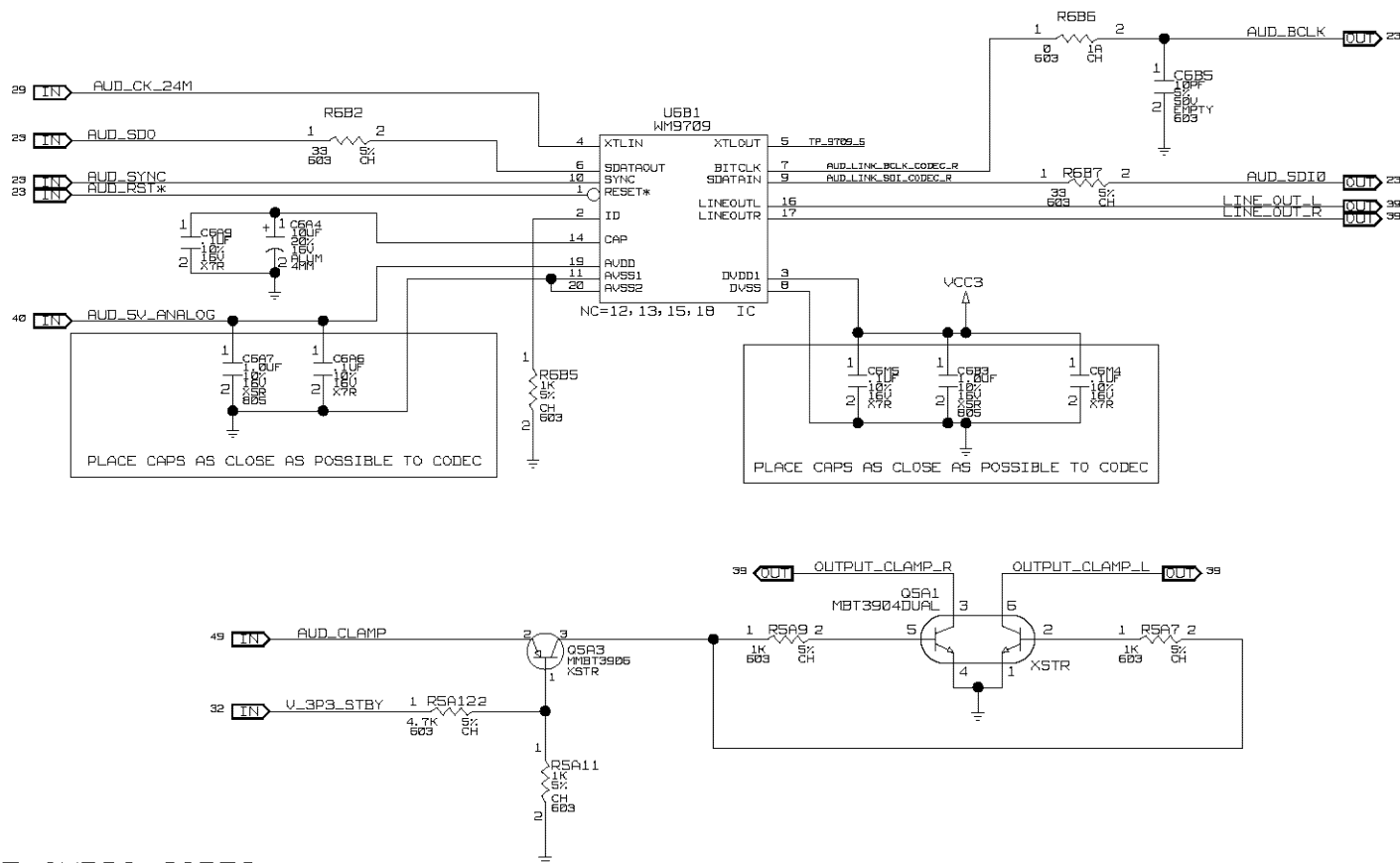
CAD NOTE:
CONNECT THE GND
ON C6F101 TO PIN 2
OF U6F100, BEFORE
VIA TO GND



[PAGE_TITLE=IDE]

DRAWING
DUT/APP. SCH. 1: 37
Fri May 03 11:23:59 2002

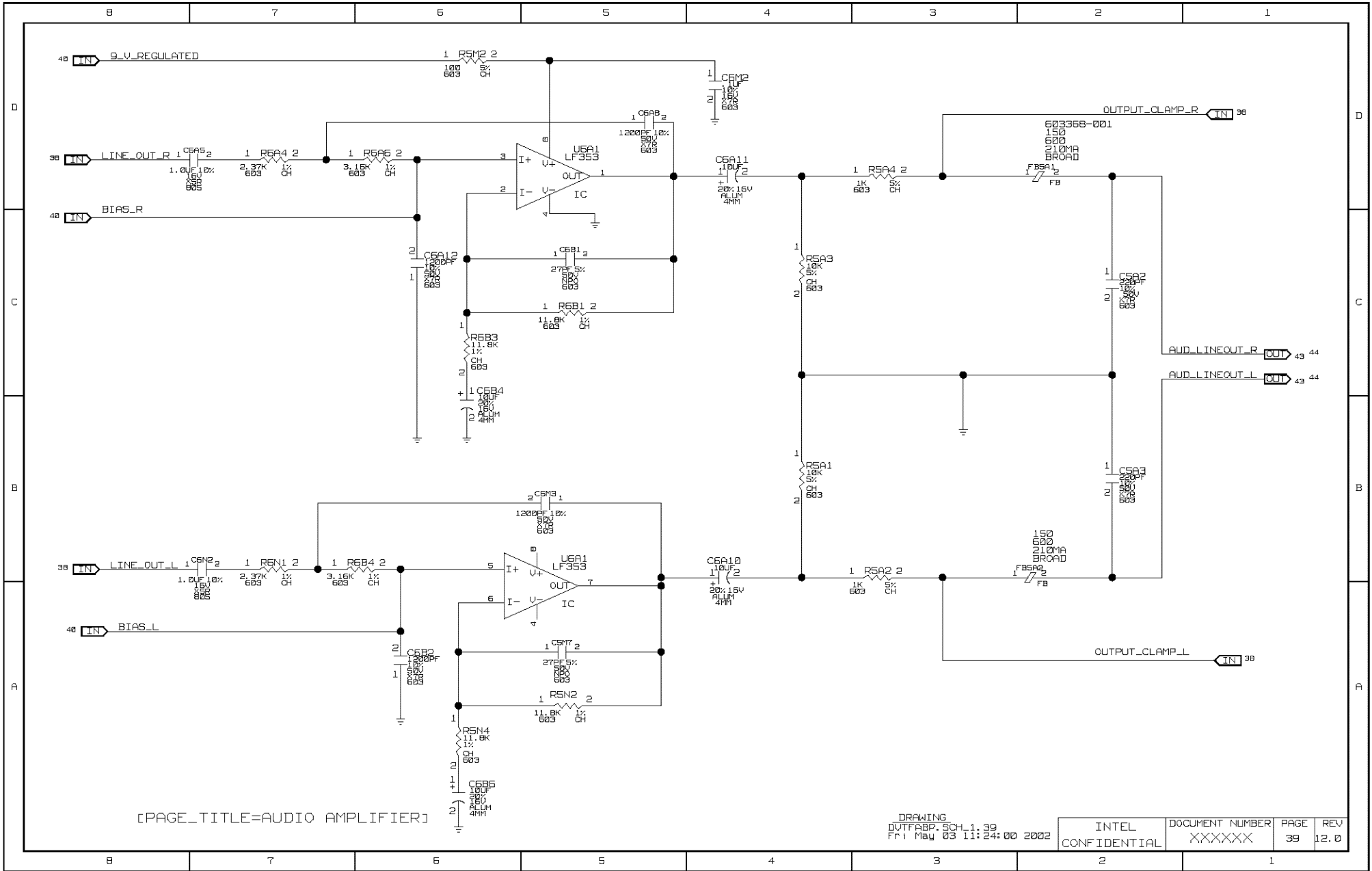
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	37	12.0

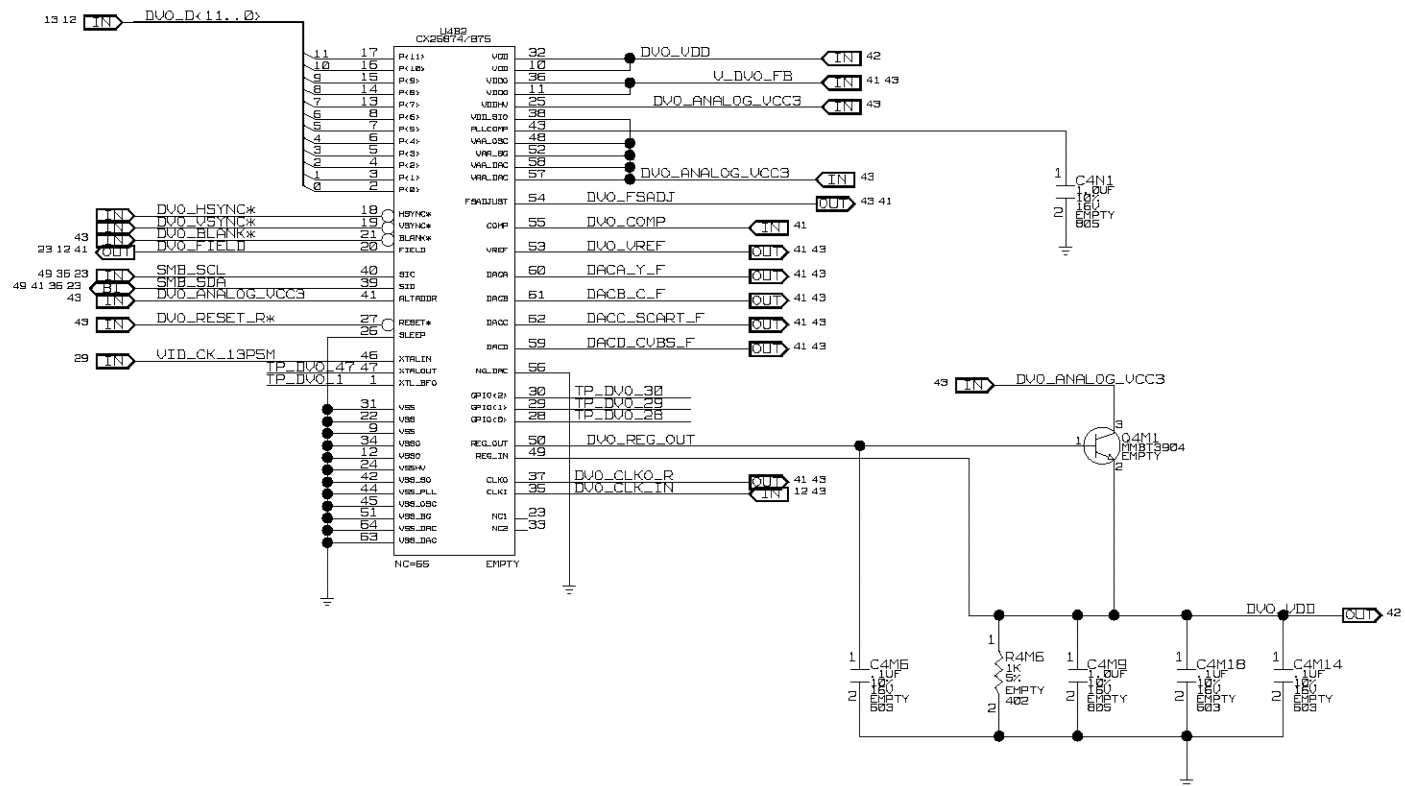


[PAGE_TITLE=AUDIO CODEC]

DRAWING
OUTFABP_SCH.1_38
Fri May 03 11:23:59 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	38	12.0

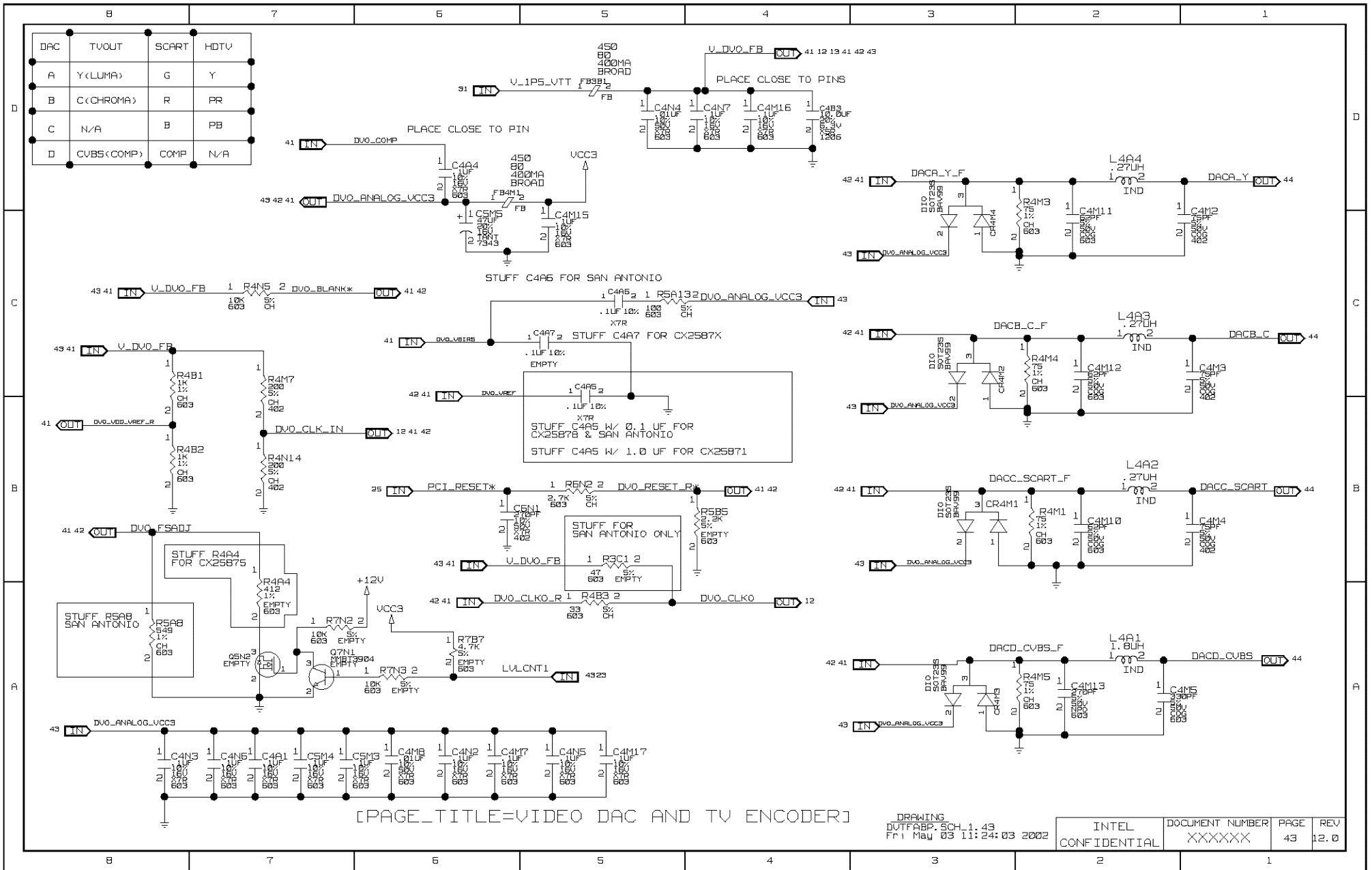


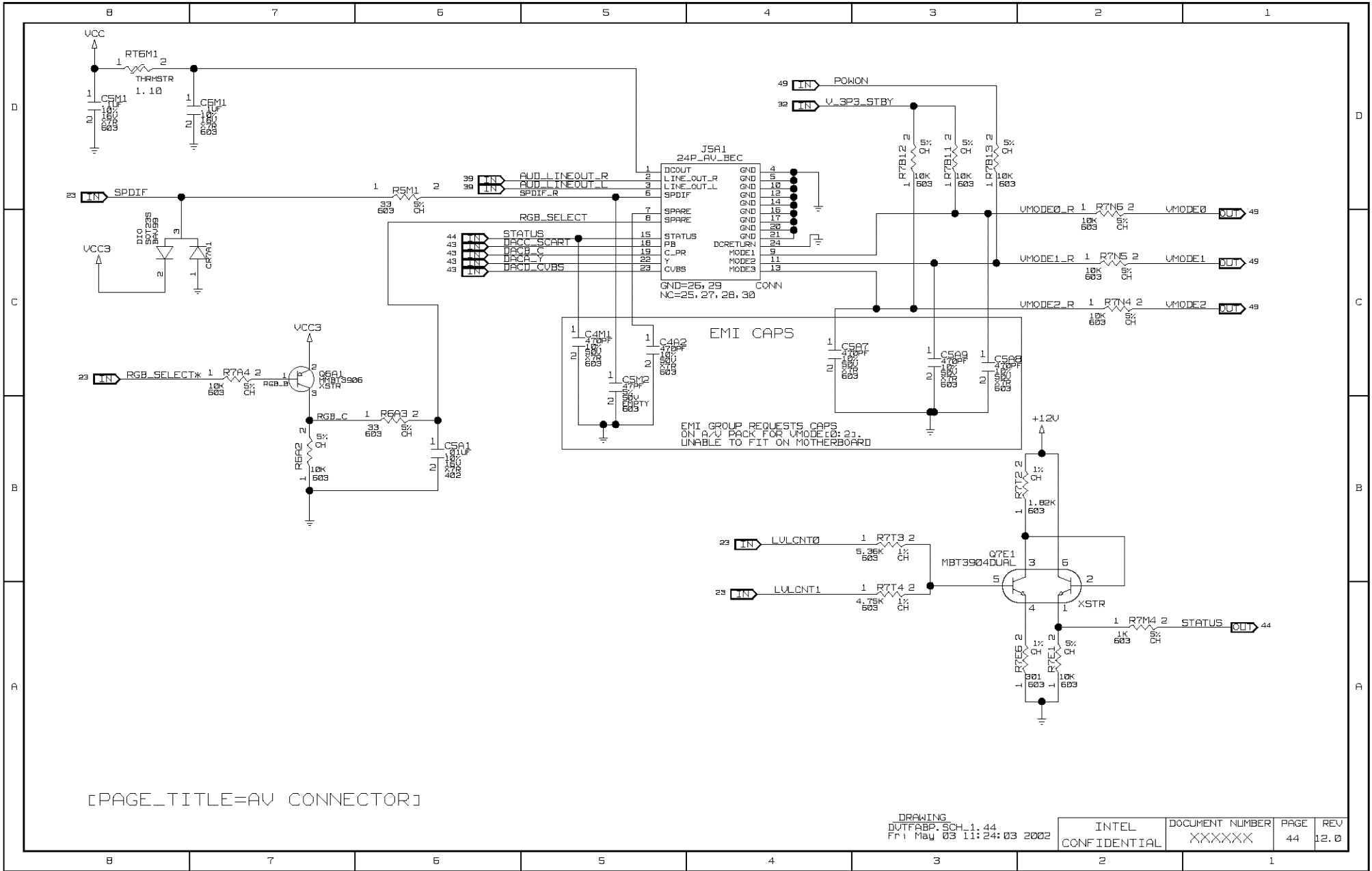


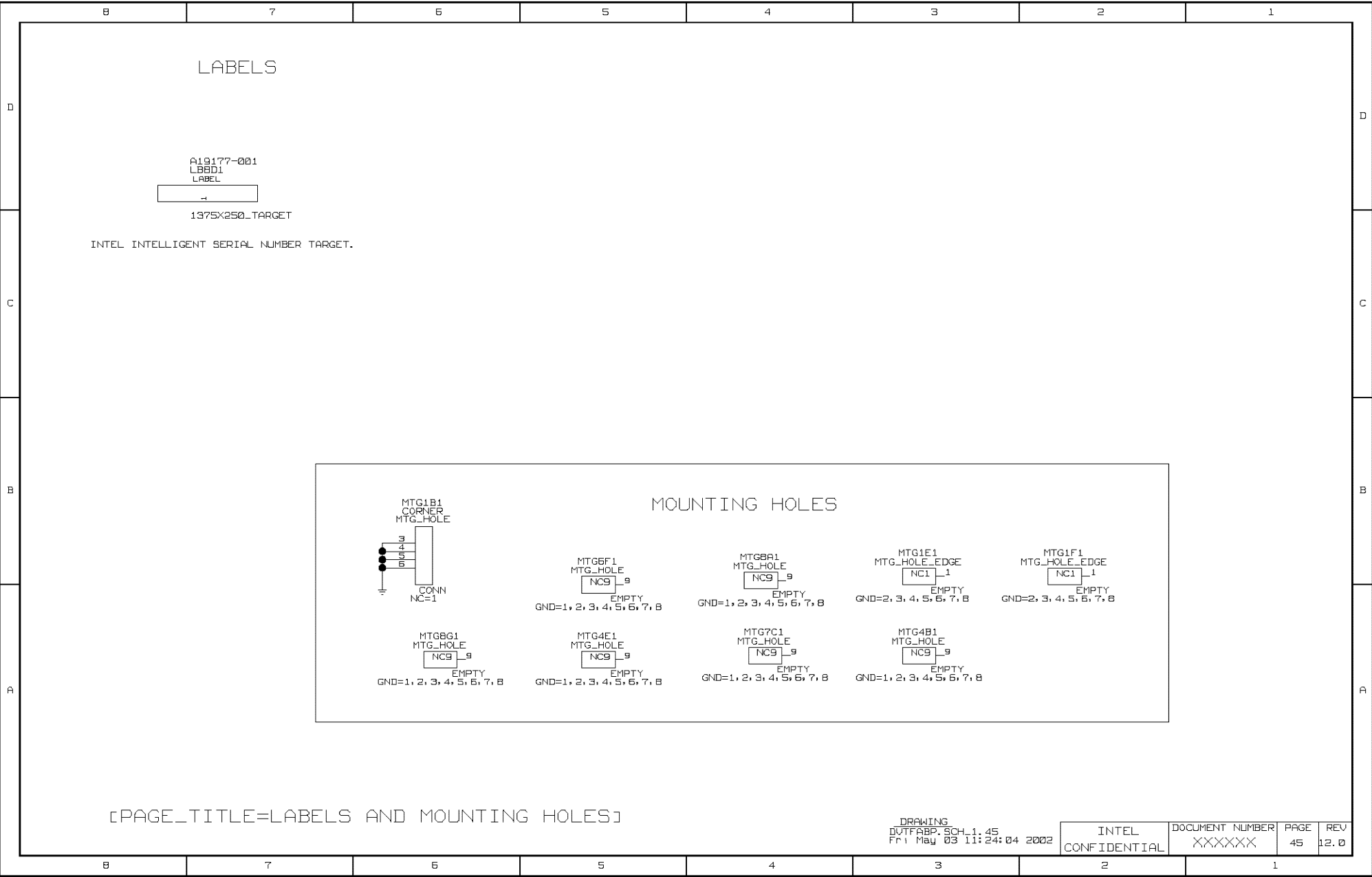
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OUTFABP, SCH 1.42
Fri May 03 11:24:02 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 42	REV 12.0
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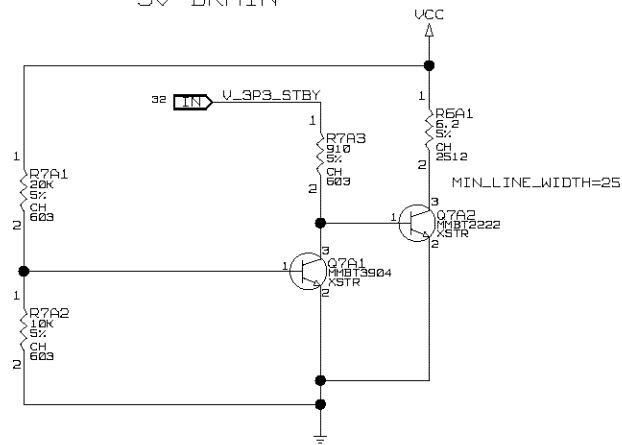
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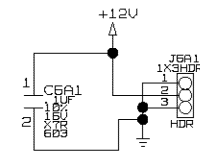


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DUTFABP.SCH_1.45
Fri May 03 11:24:05 2002

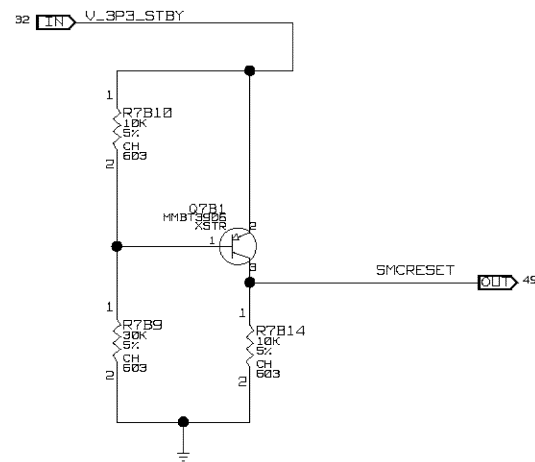
5V DRAIN



NV2A FAN HEADER



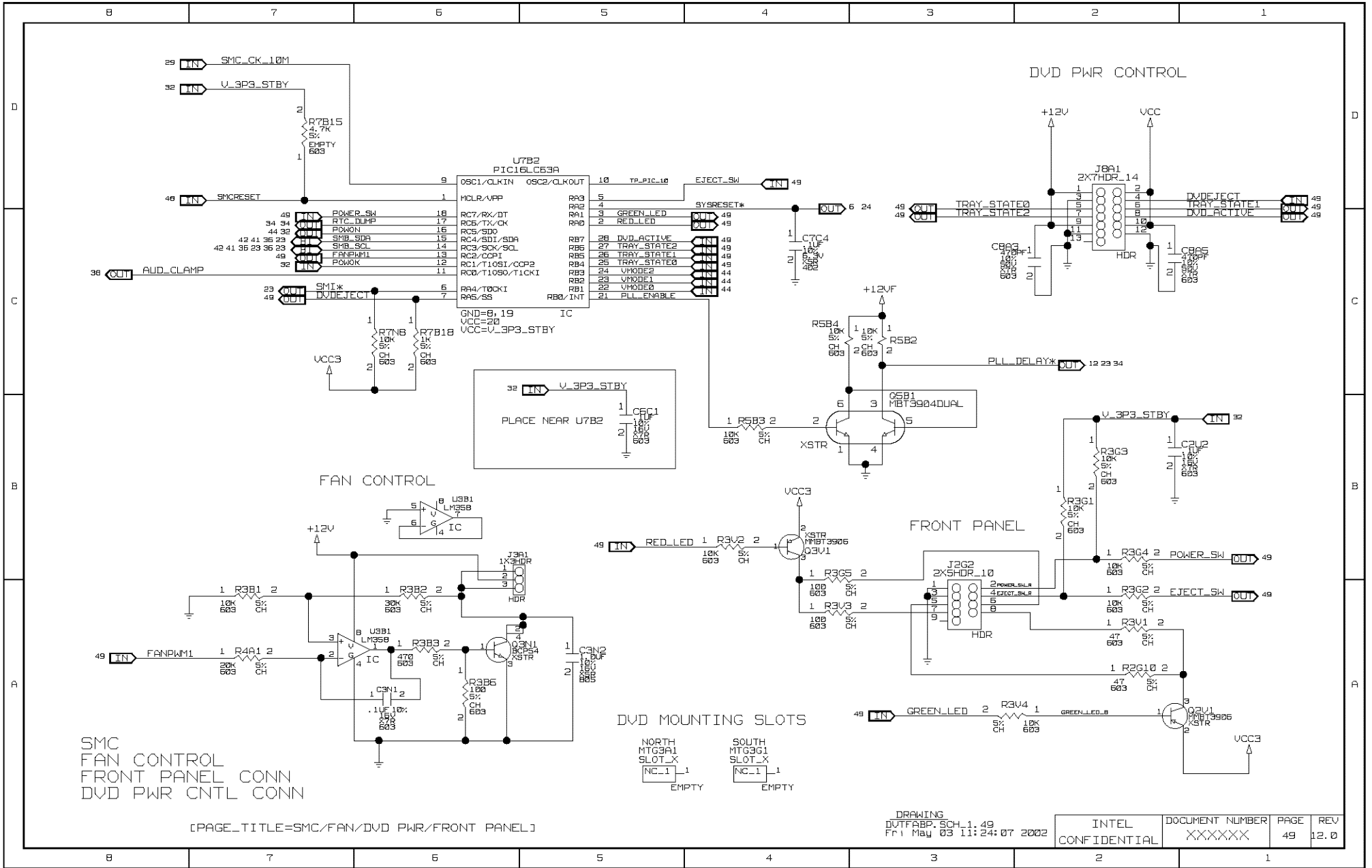
SMC BROWN OUT



[PAGE_TITLE=NV2A FAN/5V DRAIN/BROWN OUT]

DRAWING
OUTFABP. SCH.1:48
Fri May 03 11:24:06 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	48	12.0



MCPX MUXED PIN ASSIGNMENT

BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME	BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME
A5	IDE_ADDR_S0	TRST0	Y20	PCI_AD0	XBUS_A23
E6	IDE_ADDR_S1	RESERVED	Y19	PCI_AD1	XBUS_A22
B5	IDE_ADDR_S2	TRST1	AA19	PCI_AD2	XBUS_A21
C5	IDE_CS1_S*	RESERVED	AB17	PCI_AD3	XBUS_A20
B4	IDE_CS3_S*	RESERVED	AA17	PCI_AD4	XBUS_OE*
AA6	IDE_DACK_S*	TDI0	Y17	PCI_AD5	XBUS_WE*
BB	IDE_DATA_S0	TD01	V17	PCI_AD6	RESERVED
C8	IDE_DATA_S1	RESERVED	AA16	PCI_AD7	XBUS_D07
D8	IDE_DATA_S2	RESERVED	V16	PCI_AD8	XBUS_A19
B9	IDE_DATA_S3	TCK1	AB15	PCI_AD9	XBUS_A14
D9	IDE_DATA_S4	RESERVED	AA15	PCI_AD10	XBUS_A15
B10	IDE_DATA_S5	TMS1	Y15	PCI_AD11	XBUS_D06
E10	IDE_DATA_S6	RESERVED	W15	PCI_AD12	XBUS_A16
B11	IDE_DATA_S7	TDE1*	V15	PCI_AD13	XBUS_A17
A11	IDE_DATA_S8	TDE0*	AB14	PCI_AD14	XBUS_D04
E11	IDE_DATA_S9	RESERVED	AA14	PCI_AD15	XBUS_A13
C10	IDE_DATA_S10	RESERVED	Y11	PCI_AD16	XBUS_D03
E9	IDE_DATA_S11	RESERVED	W11	PCI_AD17	XBUS_CE*
A9	IDE_DATA_S12	TMS0	V11	PCI_AD18	XBUS_A12
C9	IDE_DATA_S13	RESERVED	AA10	PCI_AD19	XBUS_A8
E8	IDE_DATA_S14	RESERVED	Y10	PCI_AD20	XBUS_D02
AB	IDE_DATA_S15	TCK0	V10	PCI_AD21	XBUS_A10
E7	IDE_DR0_S	RESERVED	AB9	PCI_AD22	XBUS_A6
BB	IDE_INTR_S	TDI1	AA9	PCI_AD23	XBUS_D00
B7	IDE_IOR_S*	TD00	W9	PCI_AD24	XBUS_D01
C7	IDE_IOW_S*	RESERVED	V9	PCI_AD25	XBUS_A8
C6	IDE_RDY_S	RESERVED	AA8	PCI_AD26	XBUS_A3
			Y8	PCI_AD27	XBUS_A4
			W8	PCI_AD28	XBUS_A0
Y21	PCI_GNT0*	RESERVED	V8	PCI_AD29	XBUS_A6
Y18	PCI_GNT1*	RESERVED	V7	PCI_AD30	XBUS_A2
AA13	PCI_GNT2*	RESERVED	V6	PCI_AD31	XBUS_A1

BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME	BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME
Y7	PCI_GNT3*	RESERVED	Y16	PCI_CBE0*	XBUS_A18
Y6	PCI_GNT4*	RESERVED	W14	PCI_CBE1*	XBUS_D05
V12	PCI_IRDY*	RESERVED	AA11	PCI_CBE2*	XBUS_A11
Y14	PCI_PAR	RESERVED	Y9	PCI_CBE3*	XBUS_A7
Y13	PCI_PERR*	RESERVED	Y12	PCI_DEVEL*	RESERVED
AA20	PCI_RE00*	RESERVED	AB11	PCI_FRAME*	RESERVED
AA18	PCI_RE01*	RESERVED	V14	PCI_SERR*	RESERVED
AA12	PCI_RE02*	RESERVED	V13	PCI_STOP*	RESERVED
AA7	PCI_RE03*	RESERVED	W12	PCI_TRDY*	RESERVED
AA6	PCI_RE04*	RESERVED			

VOLTAGE RAILS

RAIL	TYPICAL (V)	
V_CPUCORE	1.7V (CPU DEPENDENT)	
VCC	5V	
VCC3	3.3V	
V_3P3_STBY	3.3V STANDBY	
V_2P5	2.65V	
V_1P5	1.65V	
V_1P5_VTT	1.5V	
V_1P25_MEMVTT	1.325V	

[PAGE_TITLE=MCPX MUXED PIN ASSIGNMENT]

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	8	7	6	5	4	3	2	1	
D	*** Signal Cross-Reference *** --- for the entire design ---		EJECT_SW 49A1 49D4 EJECT_SW_R 49A3 FANPM1 49C7 49A6 GREEN_LED 49C4 49A3 GREEN_LED_B 49A2 HDI_R_PDD(15..0) 37C3 HLAW(31..3) 5D3 11D5 HLA20H* 24D5 5B3 HLA20M_R* 5B5 HLADS* 6C2 11C6 HLBNS* 6B5 11C6 HLBPRI* 11C6 6B5 HLCPU_RST* 11C5 24D5 HLCPU_RST_R* 11C4 6C7 HLD(63..0) 5D7 11D8 HLOBSY* 6B2 11C6 HLOFER* 11C6 6B2 HLDORDY* 6B2 11C6 HLFER* 5B3 24D5 HLHIT* 6C2 11C6 HLHIT* 6B2 11B6 HLIGNE* 24D5 5B3 HLINIT* 6C5 HLINT* 24D5 6B7 HLINTA_R 6B5 HLOCK* 6B5 11B6 HLNMI 24D5 6B7 HLNMI_R 6B5 HLPREQ* 10B2 5B4 HLREQ(4..0) 6B5 11B6 HLRS(2..0) 11B5 6B2 HLSMI* 6A1 6B6 HLSMI_R* 24D5 6A3 HLTCK 10B7 5B4 HLTDI 10B2 5B4 HLTHERM 7C7 36A3 36C4 HLTHERM_P 36B3 36C4 7C7 HLTMS 10B7 5B4 HLTRODY* 11B6 6B2 HLTRST* 10B2 5B4 HLVID_0 26B8 HLVID_1 26B8 HLVID_2 26B8 HLVID_3 26B8 ICS_50 29A6 29D7 ICS_51 29A6 29D7 ICS_SEL 29A6 29D7 IDECSEL 37A2 IDE_IRO14_R 37B4 IDE_PDA(2..0) 23D4 37A6 37B6 IDE_PDA_R(2..0) 37A4 37B4 IDE_PDC31* 23D4 37A6 IDE_PDC31_R* 37A4 IDE_PDC33* 23D4 37A6 IDE_PDC33_R* 37A4 IDE_PDD(15..0) 23D4 37D5 IDE_PDDACK* 23D4 37B6 IDE_PDDACK_R* 37B4 IDE_PDRREQ 37B6 23D4 IDE_PDRREQ_R 37B5 IDE_PDIOR* 23D4 37B6 IDE_PDIOR_R* 37B5 IDE_PDIOW* 23D4 37B6 IDE_PDIOW_R* 37B5 IDEPINTR 37B6 23D4 IDEPPIORDY 37A6 23D4 IDEPRI_RST_R* 37B3 KBRSTIN* 24C6 LAN_CLK_25M 29D2 35B6 LAN_CLK_25M_R 29D6		LAN_CLK_2_5M_RX 35C1 23B7 LAN_CLK_2_5M_RX_R 35C3 LAN_CLK_2_5M_TX 35B1 23B7 LAN_CLK_2_5M_TX_R 35B3 LAN_CT 35B3 36B6 LAN_CT_R 36B7 LAN_MII_COL 35B1 23B7 LAN_MII_CRS 35C1 23B7 LAN_MII_CRS_R 35C3 LAN_MII_RX_DV 35C1 23B7 LAN_MII_RX_DV_R 35C3 LAN_MII_RXLER 35C1 23B7 LAN_MII_RXLER_R 35C3 LAN_MII_TX_EN 23B7 35B1 LAN_RD_N 36C8 35C3 LAN_RD_P 36C8 35C3 LAN_TD_N 35B3 36C8 LAN_TD_N_R 36D7 LAN_TD_P 35B3 36D8 LAN_TD_P_R 36D8 LDT_RESET* 12A4 24A5 LDT_RXD(6..0) 24A5 12B5 LDT_RXD(6..0) 24A6 12C4 LDT_RX_CLK 24A7 12B2 LDT_RX_CLK* 24A5 12B2 LDT_TXD(6..0) 12B4 24B5 LDT_TXD(6..0) 12C4 24B6 LDT_TX_CLK 12B2 24A7 LDT_TX_CLK* 12B2 24A5 LINE_OUT_L 36C2 36B6 LINE_OUT_R 36C2 36D8 LVL_CNT0 23C4 44B4 LVL_CNT1 23C4 43A5 44A4 L_AD(3..0) 23D7 23A4 25C5 L_FRAME* 23D7 23A3 L_SERIO 23A2 23D8 MCPX_TCK0 24C5 25B5 MCPX_TCK1 24C5 25B5 MCPX_TOE0 24C5 25C5 MCPX_TOE1 24C5 25C5 MCPX_TOI0 24C5 25C5 MCPX_TOI1 24C5 25C5 MCPX_THS0 24C5 25C5 MCPX_THS1 24C5 25C5 MCPX_TRST0 24C5 25B5 MCPX_TRST1 24C5 25B5 MCP_SPB_DELAY 23A7 MCP_VDD_PULL 23A5 23B4 MII_MDC 23B6 35C7 MII_MDIO 23B7 35C8 MII_RXD(3..0) 35C8 23B7 MII_TXD(3..0) 23B7 23D2 35C7 MLAB_CKE 14A4 15A4 MLA_ADDR(13..0) 11D4 14D7 MLA_CAS* 11C4 14B2 14B5 MLA_CLK 11C4 14A4 MLA_CLK* 11C2 14A4 MLA_CS(1..0) 11C5 14B2 14B7 MLA_DATA(31..0) 11D1 14D7 18D4 18D5 MLA_DQM(3..0) 11D4 18B4 14C2 14C7 MLA_DQS 11C4 14A4 18C3 MLA_RAS* 11C4 14B2 14B5 MLA_WE* 11C4 14B2 14B5 MLB_ADDR(13..0) 11B4 15D7 MLB_CAS* 11B3 15B2 15B7 MLB_CLK 11B3 15A4 MLB_CLK* 11A1 15A4 MLB_CS(1..0) 11A5 15B2 15B7 MLB_DATA(31..0) 11B1 15D7 18C4 18D1 MLB_DQM(3..0) 11B4 18A4 15C2 15C7		MLB_DQS 11A3 15A4 16A3 MLB_RAS* 11A3 15B2 15B7 MLB_WE* 11A3 15B2 15B7 MLC_CKE 16A4 17A4 MLC_ADDR(13..0) 12D6 16D7 MLC_CAS* 12C7 16B2 16B7 MLC_CLK 12C7 16A4 MLC_CLK* 12B5 16A4 MLC_CS(1..0) 12C8 16B2 16B7 MLC_DATA(31..0) 12D5 16D7 19D4 19D6 MLC_DQM(3..0) 12C8 16B4 16C2 16C7 MLC_DQS 12C7 16A4 19B3 MLC_RAS* 12C7 16B2 16B7 MLC_WE* 12C7 16C2 16C7 MLD_ADDR(13..0) 12B6 17D7 MLD_CAS* 12A7 17B2 17B7 MLD_CLK 12A7 17A4 MLD_CLK* 12A5 17A4 MLD_CS(1..0) 12A6 17B2 17B7 MLD_DATA(31..0) 12B5 17D7 19C4 19D1 MLD_DQM(3..0) 12A6 19A4 17C2 17C7 MLD_DQS 12A7 17A4 19A3 MLD_RAS* 12A7 17B2 17B7 MLD_WE* 12A7 17B2 17B7 MLVREF_0 14A3 14B7 15A2 15A7 MLVREF_1 15A3 15B8 17A2 17A7 NB_CLK_13PSM 26D1 11B5 NB_CLK_13PSM_R 29D5 NV2A_3P3_DELAY 12A2 NV2A_INTA* 12B2 24C4 NV2A_TEST 12B2 NV2A_VREF_0 11C2 NV2A_VREF_1 12C6 OUTPUT_CLAMP_L 39A3 39A1 OUTPUT_CLAMP_R 39A4 39D1 P9AC 35C3 35B6 P9AC_R 35B7 P1CL 35C3 35A6 P2LI 35C3 35A6 P2LI_R 35A7 P3D0 35C3 35A6 P4R0 35C3 35A6 PCI_CLK 24C5 23A3 PCI_CLK_FB 24C6 PCI_FRAME 24A1 25D5 PCI_PULLUP 23A3 24A1 PCI_RESET* 25A5 12B2 14A7 16A7 23A4 35B6 37B5 43B6 47D3 PCI_RESET_B* 24C4 25A6 PICD0 6B7 PICD1 6B6 PLL_VDD 12A2 PLL_DELAY* 49C2 12A4 23A6 34D3 PLL_ENABLE 49C5 POWER_SH 49B1 49C7 POWER_SH_R 49B3 POWER* 32C4 29C4 29D7 49C7 POWER* 49C7 32C6 44D4 RED_LED 49C4 49B5 RGB_B 44C7 RGB_C 44B7 RGB_SELECT 44C6 RGB_SELECT* 23C4 44C6 ROM_A(19..0) 24D6 46B6 ROM_CE* 46C4 ROM_D(7..0) 24C8 46B6 ROM_LOE* 24C7 46D7 ROM_LOE_R* 46D6 ROM_WE* 24C6 45C7 ROM_WE_R* 46C7		
C	9_V_REGULATED 40C1 39D8 10_BIAS 35B3 35D4 100_BIAS 35B3 35D2 AUD_SV_ANALOG 40D1 33B4 35B7 AUD_BCLK 36C2 23C6 AUD_BCLK_R 23C7 AUD_CLK_24M 29D2 36C7 AUD_CLK_24M_R 29D5 AUD_CLAMP 49C8 36A6 AUD_LINKOUT_L 39C1 44D6 AUD_LINKOUT_R 39C1 44D6 AUD_LINK_BCLK_CODEC_R 39C4 AUD_LINK_SDI_CODEC_R 36C4 AUD_RST* 23C7 36C7 AUD_SDI0 36C2 23C7 AUD_SDI0 23C8 36C7 AUD_SYNC 23C7 36C7 BGA2_BREQ0_C6 6B4 BIAS_L 40A1 39A6 BIAS_R 40A1 39C6 CK_HL133M_CPU 11B5 6A7 CK_HL133M_CPU_BUF 6A5 6B8 CK_HL133M_CPU_R 6B5 CK_HL133M_FB 11B6 CK_HL133M_FB_R 11B6 CK_HL_PICLK 11B6 CK_HL_PICLK_R 11B4 6B5 CLK_XTAL_X1 29D7 CLK_XTAL_X2 29D7 CNFG_SEL0 25C7 23C4 CNFG_SEL1 25C7 23B4 CNFG_SEL2 25C7 23C4 CSYNC 12B2 47D6 CSYNC_1 47D6 47D4 CSYNC_2 47D6 47D5 CSYNC_3 47D6 47B5 CSYNC_4 47D6 47B5 DACAL_Y 43D1 44C6 DACAL_Y_F 41C4 42C4 43D3 DACB_C 43C1 44C6 DACB_C_F 41C4 42C4 43C3 DAC_C_SCHART 43B1 44C6 DAC_C_SCHART_F 41C4 42B4 43B3 DACD_OVB 43A1 44C6 DACD_OVB_F 41C4 42B4 43A3 DDEJECT 49C7 49D1 DDEACTIVE 49C1 49C4 DVO_ANALOG_VCC3 43D7 41B6 41C1 41C2 41C4 42B3 42C4 42C7 43A3 43A6 43B3 43C3 43C4 DVO_BLANK* 43C5 41C6 42C7 DVO_CLK0 43A4 12C2 DVO_CLK0_R 41B2 42B4 43A6 DVO_CLK_IN 12C2 43B6 41B6 42B4 DVO_COMP 41D4 42C4 43D7 DVO_DX(1..0) 12C2 13D7 41D6 42D7 DVO_FIELD 41B2 42C7 12C2 23C2 DVO_FIELD_3P3* 23B5 DVO_F9ADJ 42C4 43B8 41B4 DVO_HSYNC* 12C2 41C6 42C7 DVO_REG_OUT 42B5 DVO_RESET_R* 43B4 41B6 42B7 DVO_VIPS 41A1 41C1 41D1 DVO_VIPS 41B4 43C5 DVO_VDD 42A2 42C4 DVO_VDD_VREF_R 43B6 41B4 41C6 DVO_VREF 41B4 42C4 43C6 DVO_VSYNC* 12C2 41C6 42C7		EJECT_SW 49A1 49D4 EJECT_SW_R 49A3 FANPM1 49C7 49A6 GREEN_LED 49C4 49A3 GREEN_LED_B 49A2 HDI_R_PDD(15..0) 37C3 HLAW(31..3) 5D3 11D5 HLA20H* 24D5 5B3 HLA20M_R* 5B5 HLADS* 6C2 11C6 HLBNS* 6B5 11C6 HLBPRI* 11C6 6B5 HLCPU_RST* 11C5 24D5 HLCPU_RST_R* 11C4 6C7 HLD(63..0) 5D7 11D8 HLOBSY* 6B2 11C6 HLOFER* 11C6 6B2 HLDORDY* 6B2 11C6 HLFER* 5B3 24D5 HLHIT* 6C2 11C6 HLHIT* 6B2 11B6 HLIGNE* 24D5 5B3 HLINIT* 6C5 HLINT* 24D5 6B7 HLINTA_R 6B5 HLOCK* 6B5 11B6 HLNMI 24D5 6B7 HLNMI_R 6B5 HLPREQ* 10B2 5B4 HLREQ(4..0) 6B5 11B6 HLRS(2..0) 11B5 6B2 HLSMI* 6A1 6B6 HLSMI_R* 24D5 6A3 HLTCK 10B7 5B4 HLTDI 10B2 5B4 HLTHERM 7C7 36A3 36C4 HLTHERM_P 36B3 36C4 7C7 HLTMS 10B7 5B4 HLTRODY* 11B6 6B2 HLTRST* 10B2 5B4 HLVID_0 26B8 HLVID_1 26B8 HLVID_2 26B8 HLVID_3 26B8 ICS_50 29A6 29D7 ICS_51 29A6 29D7 ICS_SEL 29A6 29D7 IDECSEL 37A2 IDE_IRO14_R 37B4 IDE_PDA(2..0) 23D4 37A6 37B6 IDE_PDA_R(2..0) 37A4 37B4 IDE_PDC31* 23D4 37A6 IDE_PDC31_R* 37A4 IDE_PDC33* 23D4 37A6 IDE_PDC33_R* 37A4 IDE_PDD(15..0) 23D4 37D5 IDE_PDDACK* 23D4 37B6 IDE_PDDACK_R* 37B4 IDE_PDRREQ 37B6 23D4 IDE_PDRREQ_R 37B5 IDE_PDIOR* 23D4 37B6 IDE_PDIOR_R* 37B5 IDE_PDIOW* 23D4 37B6 IDE_PDIOW_R* 37B5 IDEPINTR 37B6 23D4 IDEPPIORDY 37A6 23D4 IDEPRI_RST_R* 37B3 KBRSTIN* 24C6 LAN_CLK_25M 29D2 35B6 LAN_CLK_25M_R 29D6		LAN_CLK_2_5M_RX 35C1 23B7 LAN_CLK_2_5M_RX_R 35C3 LAN_CLK_2_5M_TX 35B1 23B7 LAN_CLK_2_5M_TX_R 35B3 LAN_CT 35B3 36B6 LAN_CT_R 36B7 LAN_MII_COL 35B1 23B7 LAN_MII_CRS 35C1 23B7 LAN_MII_CRS_R 35C3 LAN_MII_RX_DV 35C1 23B7 LAN_MII_RX_DV_R 35C3 LAN_MII_RXLER 35C1 23B7 LAN_MII_RXLER_R 35C3 LAN_MII_TX_EN 23B7 35B1 LAN_RD_N 36C8 35C3 LAN_RD_P 36C8 35C3 LAN_TD_N 35B3 36C8 LAN_TD_N_R 36D7 LAN_TD_P 35B3 36D8 LAN_TD_P_R 36D8 LDT_RESET* 12A4 24A5 LDT_RXD(6..0) 24A5 12B5 LDT_RXD(6..0) 24A6 12C4 LDT_RX_CLK 24A7 12B2 LDT_RX_CLK* 24A5 12B2 LDT_TXD(6..0) 12B4 24B5 LDT_TXD(6..0) 12C4 24B6 LDT_TX_CLK 12B2 24A7 LDT_TX_CLK* 12B2 24A5 LINE_OUT_L 36C2 36B6 LINE_OUT_R 36C2 36D8 LVL_CNT0 23C4 44B4 LVL_CNT1 23C4 43A5 44A4 L_AD(3..0) 23D7 23A4 25C5 L_FRAME* 23D7 23A3 L_SERIO 23A2 23D8 MCPX_TCK0 24C5 25B5 MCPX_TCK1 24C5 25B5 MCPX_TOE0 24C5 25C5 MCPX_TOE1 24C5 25C5 MCPX_TOI0 24C5 25C5 MCPX_TOI1 24C5 25C5 MCPX_THS0 24C5 25C5 MCPX_THS1 24C5 25C5 MCPX_TRST0 24C5 25B5 MCPX_TRST1 24C5 25B5 MCP_SPB_DELAY 23A7 MCP_VDD_PULL 23A5 23B4 MII_MDC 23B6 35C7 MII_MDIO 23B7 35C8 MII_RXD(3..0) 35C8 23B7 MII_TXD(3..0) 23B7 23D2 35C7 MLAB_CKE 14A4 15A4 MLA_ADDR(13..0) 11D4 14D7 MLA_CAS* 11C4 14B2 14B5 MLA_CLK 11C4 14A4 MLA_CLK* 11C2 14A4 MLA_CS(1..0) 11C5 14B2 14B7 MLA_DATA(31..0) 11D1 14D7 18D4 18D5 MLA_DQM(3..0) 11D4 18B4 14C2 14C7 MLA_DQS 11C4 14A4 18C3 MLA_RAS* 11C4 14B2 14B5 MLA_WE* 11C4 14B2 14B5 MLB_ADDR(13..0) 11B4 15D7 MLB_CAS* 11B3 15B2 15B7 MLB_CLK 11B3 15A4 MLB_CLK* 11A1 15A4 MLB_CS(1..0) 11A5 15B2 15B7 MLB_DATA(31..0) 11B1 15D7 18C4 18D1 MLB_DQM(3..0) 11B4 18A4 15C2 15C7		MLB_DQS 11A3 15A4 16A3 MLB_RAS* 11A3 15B2 15B7 MLB_WE* 11A3 15B2 15B7 MLC_CKE 16A4 17A4 MLC_ADDR(13..0) 12D6 16D7 MLC_CAS* 12C7 16B2 16B7 MLC_CLK 12C7 16A4 MLC_CLK* 12B5 16A4 MLC_CS(1..0) 12C8 16B2 16B7 MLC_DATA(31..0) 12D5 16D7 19D4 19D6 MLC_DQM(3..0) 12C8 16B4 16C2 16C7 MLC_DQS 12C7 16A4 19B3 MLC_RAS* 12C7 16B2 16B7 MLC_WE* 12C7 16C2 16C7 MLD_ADDR(13..0) 12B6 17D7 MLD_CAS* 12A7 17B2 17B7 MLD_CLK 12A7 17A4 MLD_CLK* 12A5 17A4 MLD_CS(1..0) 12A6 17B2 17B7 MLD_DATA(31..0) 12B5 17D7 19C4 19D1 MLD_DQM(3..0) 12A6 19A4 17C2 17C7 MLD_DQS 12A7 17A4 19A3 MLD_RAS* 12A7 17B2 17B7 MLD_WE* 12A7 17B2 17B7 MLVREF_0 14A3 14B7 15A2 15A7 MLVREF_1 15A3 15B8 17A2 17A7 NB_CLK_13PSM 26D1 11B5 NB_CLK_13PSM_R 29D5 NV2A_3P3_DELAY 12A2 NV2A_INTA* 12B2 24C4 NV2A_TEST 12B2 NV2A_VREF_0 11C2 NV2A_VREF_1 12C6 OUTPUT_CLAMP_L 39A3 39A1 OUTPUT_CLAMP_R 39A4 39D1 P9AC 35C3 35B6 P9AC_R 35B7 P1CL 35C3 35A6 P2LI 35C3 35A6 P2LI_R 35A7 P3D0 35C3 35A6 P4R0 35C3 35A6 PCI_CLK 24C5 23A3 PCI_CLK_FB 24C6 PCI_FRAME 24A1 25D5 PCI_PULLUP 23A3 24A1 PCI_RESET* 25A5 12B2 14A7 16A7 23A4 35B6 37B5 43B6 47D3 PCI_RESET_B* 24C4 25A6 PICD0 6B7 PICD1 6B6 PLL_VDD 12A2 PLL_DELAY* 49C2 12A4 23A6 34D3 PLL_ENABLE 49C5 POWER_SH 49B1 49C7 POWER_SH_R 49B3 POWER* 32C4 29C4 29D7 49C7 POWER* 49C7 32C6 44D4 RED_LED 49C4 49B5 RGB_B 44C7 RGB_C 44B7 RGB_SELECT 44C6 RGB_SELECT* 23C4 44C6 ROM_A(19..0) 24D6 46B6 ROM_CE* 46C4 ROM_D(7..0) 24C8 46B6 ROM_LOE* 24C7 46D7 ROM_LOE_R* 46D6 ROM_WE* 24C6 45C7 ROM_WE_R* 46C7		
B	9_V_REGULATED 40C1 39D8 10_BIAS 35B3 35D4 100_BIAS 35B3 35D2 AUD_SV_ANALOG 40D1 33B4 35B7 AUD_BCLK 36C2 23C6 AUD_BCLK_R 23C7 AUD_CLK_24M 29D2 36C7 AUD_CLK_24M_R 29D5 AUD_CLAMP 49C8 36A6 AUD_LINKOUT_L 39C1 44D6 AUD_LINKOUT_R 39C1 44D6 AUD_LINK_BCLK_CODEC_R 39C4 AUD_LINK_SDI_CODEC_R 36C4 AUD_RST* 23C7 36C7 AUD_SDI0 36C2 23C7 AUD_SDI0 23C8 36C7 AUD_SYNC 23C7 36C7 BGA2_BREQ0_C6 6B4 BIAS_L 40A1 39A6 BIAS_R 40A1 39C6 CK_HL133M_CPU 11B5 6A7 CK_HL133M_CPU_BUF 6A5 6B8 CK_HL133M_CPU_R 6B5 CK_HL133M_FB 11B6 CK_HL133M_FB_R 11B6 CK_HL_PICLK 11B6 CK_HL_PICLK_R 11B4 6B5 CLK_XTAL_X1 29D7 CLK_XTAL_X2 29D7 CNFG_SEL0 25C7 23C4 CNFG_SEL1 25C7 23B4 CNFG_SEL2 25C7 23C4 CSYNC 12B2 47D6 CSYNC_1 47D6 47D4 CSYNC_2 47D6 47D5 CSYNC_3 47D6 47B5 CSYNC_4 47D6 47B5 DACAL_Y 43D1 44C6 DACAL_Y_F 41C4 42C4 43D3 DACB_C 43C1 44C6 DACB_C_F 41C4 42C4 43C3 DAC_C_SCHART 43B1 44C6 DAC_C_SCHART_F 41C4 42B4 43B3 DACD_OVB 43A1 44C6 DACD_OVB_F 41C4 42B4 43A3 DDEJECT 49C7 49D1 DDEACTIVE 49C1 49C4 DVO_ANALOG_VCC3 43D7 41B6 41C1 41C2 41C4 42B3 42C4 42C7 43A3 43A6 43B3 43C3 43C4 DVO_BLANK* 43C5 41C6 42C7 DVO_CLK0 43A4 12C2 DVO_CLK0_R 41B2 42B4 43A6 DVO_CLK_IN 12C2 43B6 41B6 42B4 DVO_COMP 41D4 42C4 43D7 DVO_DX(1..0) 12C2 13D7 41D6 42D7 DVO_FIELD 41B2 42C7 12C2 23C2 DVO_FIELD_3P3* 23B5 DVO_F9ADJ 42C4 43B8 41B4 DVO_HSYNC* 12C2 41C6 42C7 DVO_REG_OUT 42B5 DVO_RESET_R* 43B4 41B6 42B7 DVO_VIPS 41A1 41C1 41D1 DVO_VIPS 41B4 43C5 DVO_VDD 42A2 42C4 DVO_VDD_VREF_R 43B6 41B4 41C6 DVO_VREF 41B4 42C4 43C6 DVO_VSYNC* 12C2 41C6 42C7		EJECT_SW 49A1 49D4 EJECT_SW_R 49A3 FANPM1 49C7 49A6 GREEN_LED 49C4 49A3 GREEN_LED_B 49A2 HDI_R_PDD(15..0) 37C3 HLAW(31..3) 5D3 11D5 HLA20H* 24D5 5B3 HLA20M_R* 5B5 HLADS* 6C2 11C6 HLBNS* 6B5 11C6 HLBPRI* 11C6 6B5 HLCPU_RST* 11C5 24D5 HLCPU_RST_R* 11C4 6C7 HLD(63..0) 5D7 11D8 HLOBSY* 6B2 11C6 HLOFER* 11C6 6B2 HLDORDY* 6B2 11C6 HLFER* 5B3 24D5 HLHIT* 6C2 11C6 HLHIT* 6B2 11B6 HLIGNE* 24D5 5B3 HLINIT* 6C5 HLINT* 24D5 6B7 HLINTA_R 6B5 HLOCK* 6B5 11B6 HLNMI 24D5 6B7 HLNMI_R 6B5 HLPREQ* 10B2 5B4 HLREQ(4..0) 6B5 11B6 HLRS(2..0) 11B5 6B2 HLSMI* 6A1 6B6 HLSMI_R* 24D5 6A3 HLTCK 10B7 5B4 HLTDI 10B2 5B4 HLTHERM 7C7 36A3 36C4 HLTHERM_P 36B3 36C4 7C7 HLTMS 10B7 5B4 HLTRODY* 11B6 6B2 HLTRST* 10B2 5B4 HLVID_0 26B8 HLVID_1 26B8 HLVID_2 26B8 HLVID_3 26B8 ICS_50 29A6 29D7 ICS_51 29A6 29D7 ICS_SEL 29A6 29D7 IDECSEL 37A2 IDE_IRO14_R 37B4 IDE_PDA(2..0) 23D4 37A6 37B6 IDE_PDA_R(2..0) 37A4 37B4 IDE_PDC31* 23D4 37A6 IDE_PDC31_R* 37A4 IDE_PDC33* 23D4 37A6 IDE_PDC33_R* 37A4 IDE_PDD(15..0) 23D4 37D5 IDE_PDDACK* 23D4 37B6 IDE_PDDACK_R* 37B4 IDE_PDRREQ 37B6 23D4 IDE_PDRREQ_R 37B5 IDE_PDIOR* 23D4 37B6 IDE_PDIOR_R* 37B5 IDE_PDIOW* 23D4 37B6 IDE_PDIOW_R* 37B5 IDEPINTR 37B6 23D4 IDEPPIORDY 37A6 23D4 IDEPRI_RST_R* 37B3 KBRSTIN* 24C6 LAN_CLK_25M 29D2 35B6 LAN_CLK_25M_R 29D6		LAN_CLK_2_5M_RX 35C1 23B7 LAN_CLK_2_5M_RX_R 35C3 LAN_CLK_2_5M_TX 35B1 23B7 LAN_CLK_2_5M_TX_R 35B3 LAN_CT 35B3 36B6 LAN_CT_R 36B7 LAN_MII_COL 35B1 23B7 LAN_MII_CRS 35C1 23B7 LAN_MII_CRS_R 35C3 LAN_MII_RX_DV 35C1 23B7 LAN_MII_RX_DV_R 35C3 LAN_MII_RXLER 35C1 23B7 LAN_MII_RXLER_R 35C3 LAN_MII_TX_EN 23B7 35B1 LAN_RD_N 36C8 35C3 LAN_RD_P 36C8 35C3 LAN_TD_N 35B3 36C8 LAN_TD_N_R 36D7 LAN_TD_P 35B3 36D8 LAN_TD_P_R 36D8 LDT_RESET* 12A4 24A5 LDT_RXD(6..0) 24A5 12B5 LDT_RXD(6..0) 24A6 12C4 LDT_RX_CLK 24A7 12B2 LDT_RX_CLK* 24A5 12B2 LDT_TXD(6..0) 12B4 24B5 LDT_TXD(6..0) 12C4 24B6 LDT_TX_CLK 12B2 24A7 LDT_TX_CLK* 12B2 24A5 LINE_OUT_L 36C2 36B6 LINE_OUT_R 36C2 36D8 LVL_CNT0 23C4 44B4 LVL_CNT1 23C4 43A5 44A4 L_AD(3..0) 23D7 23A4 25C5 L_FRAME* 23D7 23A3 L_SERIO 23A2 23D8 MCPX_TCK0 24C5 25B5 MCPX_TCK1 24C5 25B5 MCPX_TOE0 24C5 25C5 MCPX_TOE1 24C5 25C5 MCPX_TOI0 24C5 25C5 MCPX_TOI1 24C5 25C5 MCPX_THS0 24C5 25C5 MCPX_THS1 24C5 25C5 MCPX_TRST0 24C5 25B5 MCPX_TRST1 24C5 25B5 MCP_SPB_DELAY 23A7 MCP_VDD_PULL 23A5 23B4 MII_MDC 23B6 35C7 MII_MDIO 23B7 35C8 MII_RXD(3..0) 35C8 23B7 MII_TXD(3..0) 23B7 23D2 35C7 MLAB_CKE 14A4 15A4 MLA_ADDR(13..0) 11D4 14D7 MLA_CAS* 11C4 14B2 14B5 MLA_CLK 11C4 14A4 MLA_CLK* 11C2 14A4 MLA_CS(1..0) 11C5 14B2 14B7 MLA_DATA(31..0) 11D1 14D7 18D4 18D5 MLA_DQM(3..0) 11D4 18B4 14C2 14C7 MLA_DQS 11C4 14A4 18C3 MLA_RAS* 11C4 14B2 14B5 MLA_WE* 11C4 14B2 14B5 MLB_ADDR(13..0) 11B4 15D7 MLB_CAS* 11B3 15B2 15B7 MLB_CLK 11B3 15A4 MLB_CLK* 11A1 15A4 MLB_CS(1..0) 11A5 15B2 15B7 MLB_DATA(31..0) 11B1 15D7 18C4 18D1 MLB_DQM(3..0) 11B4 18A4 15C2 15C7		MLB_DQS 11A3 15A4 16A3 MLB_RAS* 11A3 15B2 15B7 MLB_WE* 11A3 15B2 15B7 MLC_CKE 16A4 17A4 MLC_ADDR(13..0) 12D6 16D7 MLC_CAS* 12C7 16B2 16B7 MLC_CLK 12C7 16A4 MLC_CLK* 12B5 16A4 MLC_CS(1..0) 12C8 16B2 16B7 MLC_DATA(31..0) 12D5 16D7 19D4 19D6 MLC_DQM(3..0) 12C8 16B4 16C2 16C7 MLC_DQS 12C7 16A4 19B3 MLC_RAS* 12C7 16B2 16B7 MLC_WE* 12C7 16C2 16C7 MLD_ADDR(13..0) 12B6 17D7 MLD_CAS* 12A7 17B2 17B7 MLD_CLK 12A7 17A4		

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	RSET_NU2Ak 12A4 RTC_DUMP 49C7 34C1 RTC_X1 23B5 RTC_X0 23B5 SB_CK_13PSM 29D2 23B4 SB_CK_13PSM_R 29D6 SMB_SCL 23B3 36D3 49C7 23A4 36B3 36C2 41B6 SMB_SDA 42C7 23A2 23B3 36B2 36B3 36D1 41B6 42C7 49C7 SMCRESET 48A3 49D7 SMC_CK_10M 29D2 49D7 SMC_CK_10M_R 29D5 SPDIF 49C7 23C4 SPDIF 23B3 44D8 SPDIF_R 44D6 SPKR_STRAP 23B5 STATUS 44A1 44C6 SYSRESET* 49C4 6B2 24D5 SYSRESET_R* 6B2 6C7 TP16_EN 26B8 26C7 TP_1032_4 36B3 TP_1032_6 36B2 TP_57B3_3 36C4 TP_BGA2_A4 5C4 TP_BGA2_A6 5C4 TP_BGA2_AA1 6C3 TP_BGA2_AA17 7C7 TP_BGA2_AA21 5B4 TP_BGA2_AB1 6C3 TP_BGA2_AB19 7B7 TP_BGA2_AC17 7B7 TP_BGA2_A09 5B4 TP_BGA2_A020 7C7 TP_BGA2_B4 5C4 TP_BGA2_C5 5C4 TP_BGA2_E6 5C4 TP_BGA2_G4 7C7 TP_BGA2_H4 7C7 TP_BGA2_P20 6B3 TP_BGA2_P21 6B3 TP_BGA2_R2 7B7 TP_BGA2_R21 6B3 TP_BGA2_T21 6B3 TP_BGA2_U19 6B3 TP_BGA2_VB1 6B3 TP_BGA2_V1B 6B3 TP_BGA2_VB0 6B3 TP_BGA2_V21 5C4 TP_BGA2_W2 6C3 TP_BGA2_W19 5B4 TP_BGA2_W21 5B4 TP_BGA2_Y1 6B3 TP_BGA2_Y2 6C3 TP_BGA2_Y21 5B4 TP_BUF24M 24A3 TP_CDRSV0 11B6 TP_CDRSV1 11B6 TP_DEBUG_GP1015 23C4 TP_DV0_1 42B6 TP_DV0_2B 42B5 TP_DV0_29 42B5 TP_DV0_30 42B5 TP_DV0_47 42B6 TP_INIT* 24D5 TP_MCPX_AA19 24D7 TP_MCPX_AB17 24D7 TP_MCPX_AB21 23C4 TP_MCPX_TD00 24C5 TP_MCPX_TD01 24C5	TP_MCPX_Y2 23B5 TP_MCPX_Y19 24D7 TP_MCPX_Y20 24D7 TP_PIC_10 49D5 TP_PRIIDE_32 37A2 TP_PRIIDE_34 37A2 TP_PRIIDE_39 37A3 TP_REFB 26B6 TP_RQMLCE* 24C7 TP_SA_GPI02 41B6 TRAY_STATE0 49C3 49C4 TRAY_STATE1 49C1 49C4 TRAY_STATE2 49C3 49C4 USBPWR_1 47D4 USBPWR_2 47C4 USBPWR_3 47C4 USBPWR_4 47B5 USB_L1 23D7 47D1 47C7 USB_L1* 23D7 47D1 47B7 USB_L1FB 47D3 USB_L1FB* 47D3 USB_L1R 47D2 USB_L2 23D7 47C1 47A7 USB_L2* 23D7 47C1 47A7 USB_L2FB 47C3 USB_L2FB* 47C3 USB_L2R 47C2 USB_L2R* 47C2 USB_L3 23D7 47B1 47A6 USB_L3* 23D7 47B1 47A6 USB_L3FB 47B3 USB_L3FB* 47B3 USB_L3R 47B2 USB_L3R* 47B2 USB_L4 23D7 47A1 47A5 USB_L4* 23C7 47A1 47A3 USB_L4FB 47A3 USB_L4FB* 47A3 USB_L4R 47A2 USB_L4R* 47A2 USB_L5 23C7 25A1 USB_L5* 23C7 25B1 USB_VREF 23C7 VIO_CK_13PSM 29D2 41A6 42B7 VIO_CK_13PSM_R 29A6 29D3 VMODE0 44C1 49C4 VMODE0_R 44C2 VMODE1 44C1 49C4 VMODE1_R 44C2 VMODE2 44C1 49C4 VMODE2_R 44C2 VREG_1PS_GATE 26B8 31D8 VREG_2PS_GATE 26B8 31B8 VREG_CON 26B5 VREG_CSP 26C5 VREG_CSP_R 26B3 VREG_FETDRVA 26C5 VREG_FETDRVA_FETDRVB_PN1 26C3 VREG_FETDRVB 26C5 VREG_PVCC 26D7 VREG_PWRG000 26B6 VREG_VCC 26D8 VREG_VCCP_R 26C2 VREG_VO_SENSE 26A4 V_1PS 26C1 12B2 22D8 24A7 24C1 29B2 34D3 V_1PS_FEEDBACK 26A4 V_1PS_VTT 31C2 5C2 6D7 7B6 7D1 7D4 7D9 9D7 1B05 11B5 11C5 22D2 24B1 24C4 26A6 43D6	V_1P25_MEMVTT 30B2 18A3 18A6 18B3 18B6 18C6 18D2 18D6 18D8 19A3 19A6 19B3 19B6 19C6 19D3 19D6 19D8 20B3 20B6 20D3 20D6 20D8 V_2P5 31B3 7B7 11A3 11A4 11B4 11C1 11C4 12A7 12C7 12D4 14A6 14B2 14B7 15A2 15A7 16A6 16B2 16B7 17A2 17A7 20B2 20B5 20B6 20D3 20D5 20D6 21C5 21D1 21D2 21D6 21D7 22D5 26A6 26B6 26C6 30B7 30C6 V_3P3_FB 29A1 29A8 29C7 V_3P3_STBY 32D8 29A6 34D7 38A6 44D4 46B5 46D7 49B1 49C5 49D7 V_SFB_FILTERED 26D3 28D7 29A4 32B4 V_BAT_RTC 34C1 23B4 V_BAT_RTC_FET 34D3 V_CLKREF 7A5 7D8 V_CPUCORE 26C1 7C4 8D3 8D7 27C6 41A3 V_DV0_FB 41B2 43D4 12C1 13C8 41D1 41D4 42C4 43B6 43C8 V_DV0_REF 12B2 V_GTLREF 7B4 7B5 7D8 V_GTLREF_1PB 11A4 11B5 V_GTLREF_MCP 24B3 24D5 V_LAN_3P3V 35A3 35C8 35D1 36B7							
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D	*** Unit Cross-Reference *** --- for the entire design ---								D
C	C1C1 CAPN 7B5 C1D1 CAPN 5A1 C1D2 CAPN 22C1 C1D3 CAPN 5A2 C1D4 CAPN 7A6 C1D5 CAPN 7A6 C1E1 CAP-P 27C4 C1F1 CAPN 26D4 C1F2 CAPN 26D4 C1G1 CAP-P 26D5 C1G2 CAPN 26D4 C1G3 CAP-P 47C5 C1G4 CAPN 47D3 C1G5 CAPN 47D4 C1G6 CAP-P 47D5 C1G7 CAPN 47C5 C1P1 CAPN 8B5 C1P2 CAPN 27B4 C1P3 CAPN 8D2 C1P4 CAPN 27B4 C1P5 CAPN 8B2 C1P6 CAPN 7A4 C1P7 CAPN 9B5 C1P8 CAPN 9B5 C1P9 CAPN 8C2 C1P10 CAPN 9A6 C1P11 CAPN 9C8 C1P12 CAPN 7A5 C1R1 CAPN 9A6 C1R2 CAPN 8C2 C1R3 CAPN 8C2 C1R4 CAPN 27B5 C1R5 CAPN 27B5 C1R6 CAPN 8B2 C1R7 CAPN 8A5 C1R8 CAPN 7A5 C1R9 CAPN 7A7 C1T1 CAPN 33D6 C2D1 CAPN 26D8 C2D2 CAPN 26B4 C2D3 CAPN 26A7 C2E1 CAPN 26D7 C2E2 CAPN 26A4 C2E3 CAP-P 27C5 C2E4 CAP-P 27C3 C2E5 CAP-P 27C3 C2E6 CAPN 32C5 C2E7 CAPN 32C6 C2F1 CAP-P 26D5 C2G1 CAPN 32B1 C2G2 CAPPDFPN 32A1 C2G3 CAPN 47C5 C2G4 CAPN 47C3 C2G5 CAPN 47C3 C2G6 CAPN 26D6 C2G7 CAPN 47D3 C2G8 CAPN 47D3 C2G9 CAPN 47D7 C2G10 CAPN 47C4 C2N1 CAP-P 31C3 C2N2 CAP-P 31C3 C2P1 CAPN 7A5 C2P2 CAPN 9B5 C2P3 CAPN 9C5 C2P4 CAPN 9B5 C2P5 CAPN 9B5 C2P6 CAPN 9B5	C2P7 CAPN 8A5 C2P8 CAPN 8D6 C2P9 CAPN 8A5 C2P10 CAPN 9C6 C2P11 CAPN 8B6 C2P12 CAPN 9C5 C2P13 CAPN 9C5 C2P14 CAPN 9C5 C2P15 CAPN 9C6 C2P16 CAPN 8D5 C2P17 CAPN 9C5 C2P18 CAPN 9C5 C2P19 CAPN 9C6 C2P20 CAPN 8B6 C2P21 CAPN 8B5 C2P22 CAPN 8B5 C2P23 CAPN 8B5 C2P24 CAPN 9A5 C2R1 CAPN 11C4 C2R2 CAPN 9C5 C2R3 CAPN 9B5 C2R4 CAPN 9B5 C2R5 CAPN 9C6 C2R6 CAP-P 7D5 C2R7 CAPN 26A7 C2T1 CAPN 26D7 C2T2 CAPN 33A4 C2U1 CAPN 26C2 C2U2 CAPN 49B1 C2V1 CAPN 32B1 C2A1 CAPN 33D5 C2B1 CAPN 11C5 C2B2 CAPPDFPN 31C6 C2B3 CAPN 31C5 C2B4 CAPN 31C4 C2B5 CAPN 31C4 C2B6 CAPN 31C4 C2B7 CAPN 22C1 C2D1 XCAP 5A6 C2D2 XCAP 5A6 C2E1 CAPN 20B5 C2E2 CAP-P 27C4 C2E3 XCAP 20A5 C2E4 CAPN 20B3 C2E5 XCAP 21D3 C2E6 XCAP 21B3 C2E7 XCAP 21C5 C2E8 XCAP 20A5 C2E9 XCAP 21D2 C2F1 XCAP 20A5 C2F2 XCAP 21D2 C2F3 CAPN 32B2 C2F4 CAPN 32B2 C2F5 XCAP 20A5 C2F6 CAPPDFPN 32A2 C2F7 XCAP 21A3 C2F8 CAPN 32B2 C2F9 CAPN 32B2 C2F10 CAPPDFPN 31B5 C2F11 CAPN 32A2 C2G1 CAPPDFPN 32A2 C2G2 CAPN 26D6 C2G3 CAPN 47B7 C2G4 CAPN 32B2 C2G5 CAPN 32B2 C2G6 CAPN 32A2 C2G7 CAPN 32B2 C2G8 CAPN 32B2 C2G9 CAPN 32C7 C2N1 CAPN 49A6	C3N2 CAPN 49A5 C3N3 CAPN 31C5 C3P1 CAPN 22D1 C3P2 CAPN 22C1 C3P3 CAPN 11A5 C3P4 CAPN 12A1 C3P5 CAPN 12A2 C3R1 CAPN 11A5 C3R2 XCAP 20A3 C3T1 XCAP 20A4 C3T2 XCAP 21C3 C3T3 XCAP 20A3 C3U1 XCAP 20A3 C3U2 XCAP 21C7 C4A1 CAPN 43A7 C4A2 CAPN 44C5 C4A3 CAPN 41C4 C4A4 CAPN 43D6 C4A5 CAPN 43C5 C4A6 CAPN 43C5 C4A7 CAPN 43C5 C4A8 CAPN 41A1 C4B1 CAPN 41A1 C4B2 CAPN 41A2 C4B3 CAPN 43D4 C4B4 CAPN 31D7 C4B5 CAPN 31D8 C4B6 CAPN 12A1 C4E1 XCAP 21D7 C4E2 XCAP 20D2 C4E3 XCAP 21B4 C4E4 XCAP 20A3 C4E5 XCAP 20C2 C4E6 XCAP 21B5 C4E7 XCAP 20A3 C4E8 XCAP 21B5 C4F1 XCAP 21C4 C4F2 XCAP 20C2 C4F3 XCAP 21A3 C4F4 XCAP 21B4 C4F5 XCAP 21A4 C4F6 CAPN 16A3 C4F7 XCAP 20C2 C4F8 XCAP 21C3 C4F9 CAP-P 30B3 C4G1 CAPPDFPN 30C3 C4G2 CAPN 30B4 C4G3 CAPN 30B5 C4G4 CAP-P 47B5 C4G5 CAPN 47B5 C4G6 CAPN 47B4 C4G7 CAPN 47B3 C4G8 CAP-P 47B5 C4G9 CAPN 47B3 C4G10 CAPN 47A3 C4G11 CAPN 47B4 C4G12 CAPN 47B5 C4G13 CAPN 47A3 C4G14 CAPN 30B5 C4H1 CAPN 44C5 C4H2 XCAP 43C1 C4H3 XCAP 43C1 C4H4 XCAP 43B1 C4H5 CAPN 43A2 C4H6 CAPN 42A4 C4H7 CAPN 43A6 C4H8 CAPN 43A6 C4H9 CAPN 42A3 C4H10 CAPN 43B2 C4H11 CAPN 43C2	C4M12 CAPN 43C2 C4M13 CAPN 43A2 C4M14 CAPN 42A2 C4M15 CAPN 43C5 C4M16 CAPN 43D4 C4M17 CAPN 43A5 C4M18 CAPN 42A3 C4N1 CAPN 42C3 C4N2 CAPN 43A6 C4N3 CAPN 43A6 C4N4 CAPN 43D5 C4N5 CAPN 43A6 C4N6 CAPN 43A7 C4N7 CAPN 43D4 C4N8 CAPN 31D8 C4N9 CAPN 31D7 C4P1 XCAP 20A3 C4P2 CAPN 12B1 C4P3 CAPN 22D3 C4P4 CAPN 22A4 C4P5 CAPN 22B4 C4P6 CAPN 22B4 C4P7 CAPN 22A4 C4P8 CAPN 22A4 C4P9 CAPN 22C3 C4P10 CAPN 22B4 C4P11 CAPN 33B6 C4P12 XCAP 22C5 C4P13 XCAP 22B5 C4P14 XCAP 22C3 C4P15 XCAP 22C5 C4P16 CAPN 22C3 C4P17 CAPN 11A6 C4P18 CAPN 22A7 C4P19 CAP-P 22C7 C4P20 CAPN 22B7 C4P21 CAPN 22C7 C4P22 XCAP 12C1 C4P23 CAPN 12C1 C4R1 CAPN 22A6 C4R2 CAPN 22B7 C4R3 XCAP 22B5 C4R4 CAPN 22C7 C4R5 CAPN 22B7 C4R6 CAPN 22C7 C4R7 XCAP 22C5 C4R8 CAPN 11A4 C4R9 XCAP 22C5 C4R10 XCAP 22A5 C4R11 XCAP 22B5 C4R12 CAPN 22D6 C4R13 CAPN 22C6 C4R14 CAPN 22C4 C4R15 CAPN 22D4 C4R16 CAPN 22B6 C4R17 CAPN 22B6 C4R18 CAPN 22C4 C4R19 CAPN 22C4 C4R20 XCAP 12D4 C4R21 XCAP 20B3 C4T1 XCAP 21C7 C4T2 XCAP 20B4 C4T3 XCAP 20A4 C4T4 XCAP 20D1 C4T5 XCAP 21B4 C4T6 XCAP 20C1 C4U1 XCAP 20A4 C4U2 XCAP 21A6 C4U3 XCAP 21B5 C4U4 XCAP 20A4	C				
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DBSF1	X_DBP40	30C2
DBSF1	X_DBP40	31B4
DBSF2	X_DBP40	34C1
DBTF1	X_DBP40	28C3
FB3B1	FERR_B0	43D5
FB3R1	FERRITE	12A1
FB4M1	FERR_B0	43D6
FB4N1	FERR_B0	41A3
FB5A1	FERR_B0	39D2
FB5A2	FERR_B0	39B2
FB6E1	FERRITE	23A6
FB7A1	FERRITE	40D8
FB7A2	FERRITE	35A6
FB8C1	FERRITE	29B5
FP2G1	LPAK4L	47C2 47D8
FP5G1	LPAK4L	47A2 47B2
J1G1	2XSHDR12	47D4
J2G1	2X10P4R	32D6
J2G2	2XSHDR10	49B3
J3A1	1X3HDR	49B5
J4G1	2XSHDR12	47B4
J5A1	24P_A/V_BEC	44D4
J6A1	1X3HDR	46D3
J7D1	2XSHDR4	29B3
J8A1	2X7HDR14	49D2
J8C1	2X20HDR20	37B3
JAT7A1	RJ45_2LED_TABUR	36A7 36B7 36D6
L1F1	INDUCTOR	26C2
L1R1	INDUCTOR	7D5
L3G1	INDUCTOR	26D5
L4A1	INDUCTOR	43A2
L4A2	INDUCTOR	43B2
L4A3	INDUCTOR	43C2
L4A4	INDUCTOR	43D2
L7F1	INDUCTOR	26C3
L7H1	INDUCTOR	36D7
L7N1	INDUCTOR	36D7
LB0D1	LABEL	45D7
MTG1B1	MTGGR_2.7	45B5
MTG1E1	STD_MTG_EDGE	45B3
MTG1F1	STD_MTG_EDGE	45B2
MTG3A1	SLOT_X	49A5
MTG3G1	SLOT_X	49A4
MTG4B1	STD_MTG_HOLE	45A3
MTG4E1	STD_MTG_HOLE	45A5
MTG6F1	STD_MTG_HOLE	45B5
MTG7C1	STD_MTG_HOLE	45A4
MTG8A1	STD_MTG_HOLE	45B4
MTG8C1	STD_MTG_HOLE	45A6
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Q2U1	FET_VREG	26C3
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Q3F1	NPV	23C3
Q3N1	BOP54	49A6
Q3V1	PNP	49B4
Q4R1	NPV	42B3
Q5A1	MBT3904DUAL	39A4
Q5A2	MBT413LT1	41A3
Q5A3	PNP	38A5
Q5B1	MBT3904DUAL	49B3
Q5F1	MBT3904DUAL	16A5
Q5M1	NPV	40B6
Q5N1	NPV	40D5
Q5N2	FET	43A7
Q5N3	FET	12A3
Q6A1	PNP	44C7
Q6C1	MBT3904DUAL	14A6
Q6F1	FET	23A7
Q7A1	NPV	48C7
Q7A2	NPV	48C6

Q7B1	PNP	48B4
Q7C1	MBT3904DUAL	44B2
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Q7F2	FET	34C2
Q7F3	PNP	34C5
Q7F4	PNP	34C5
Q7G1	FET_VREG	26C4
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Q7N1	NPV	43A7
Q7R1	MBT3904DUAL	25A7
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Q8C2	NPV	26B7
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R1B3	RESN	10C3
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R1C2	RESN	6C7
R1C3	RESN	6C5
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R1C7	RESN	6C4
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R1C9	RESN	5C3
R1C10	RESN	6C4
R1C11	RESN	7D7
R1C12	RESN	5C3
R1C13	RESN	6C5
R1C14	RESN	6C4
R1C15	RESN	6C5
R1C16	RESN	6A2
R1C17	RESN	6C5
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R1D5	RESN	6B1
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R1D8	RESN	6B6
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R1D10	RESN	7A5
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R1P2	RESN	5B4
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R1T2	GND_ISOLATION	26A5
R1T3	GND_ISOLATION	26B2
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R2D3	RESN	26A7
R2D4	RESN	26B3
R2D5	RESN	26A7
R2E1	RESN	26D8
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R2E8	RESN	26A4
R2E9	RESN	26B3
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R2G2	RESN	47D2
R2G3	RESN	47D1

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R2G5	RESN	47C2
R2G6	RESN	47C2
R2G7	RESN	47C1
R2G8	RESN	47C2
R2G9	RESN	47D7
R2G10	RESN	49A2
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R2T1	RESN	26D6
R2U1	RESN	26C2
R2U2	RESN	26C4
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R3B2	RESN	49A6
R3B3	RESN	49A6
R3B4	RESN	11C8
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R3B6	RESN	49A6
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R3G2	RESN	49A2
R3G3	RESN	49B2
R3G4	RESN	49B2
R3G5	RESN	49B4
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R3P2	RESN	11A5
R3P3	RESN	11C5
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R3V3	RESN	49A4
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R4B2	RESN	43B8
R4B3	RESN	43A5
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R4B5	RESN	13C1
R4B6	RESN	13C7
R4B7	RESN	41B2
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R4N7	RESN	13B6
R4N8	RESN	13B6
R4N9	RESN	13B6
R4N10	RESN	13C6
R4N11	RESN	13B6
R4N12	RESN	13C8

R4N13	RESN	13B6
R4N14	XRES	43B7
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R4R2	XRES	12D4
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RSB2	RESN	39B3
RSB3	RESN	39C4
RSB4	RESN	39D3
RSB5	XRES	41C2
RSB6	RESN	41B4
RSB7	RESN	39B3
RSB8	RESN	43B8
RSB9	RESN	39B4
RSA10	RESN	41A4
RSA11	RESN	39A5
RSA12	RESN	39A6
RSA13	RESN	43C5
RSB1	RESN	41C2
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RSB3	RESN	49B4
RSB4	RESN	49C4
RSB5	RESN	43B4
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RSF2	RESN	16A5
RSF3	RESN	16A3
RSF4	RESN	16A6
RSF5	RESN	16A6
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RSG2	RESN	47B2
RSG3	RESN	47B1
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RSG7	RESN	47A2
RSG8	RESN	47A1
RSG9	RESN	47A2
RSM1	RESN	44D6
RSM2	RESN	39D6
RSM3	RESN	40B3
RSM4	RESN	40B6
RSM5	RESN	40A7
RSM6	RESN	40A6
RSN1	RESN	40D3
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RSN3	RESN	40D5
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RSN7	RESN	12A1
RSP1	XRES	11C1
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RSV3	RESN	48B6
RSV4	RESN	44B7
RSV5	RESN	44B6
RSV6	RESN	39D6
RSV7	RESN	39C5
RSV8	RESN	39C6
RSV9	RESN	39C6
RSV10	RESN	39B6
RSV11	RESN	39B5
RSV12	RESN	39C3
RSV13	RESN	39C3

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	R6F4 XRES 25B4		R7D8 XRES 25D1		R8C6 RESN 37C2		RT3G1 THERMISTOR 47B6		
	R6F5 RESN 24B4		R7D9 XRES 46D5		R8D1 RESN 37B4		RT3V1 THERMISTOR 47C6		
	R6F6 RESN 24B4		R7D10 XRES 46D6		R8E1 RESN 23C3		RT3V2 THERMISTOR 47B6		
	R6F7 XRES 34C5		R7E1 RESN 44A2		R8E2 RESN 23C4		RT6M1 THERMISTOR 44D8		
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	R6H3 RESN 40B3		R7E4 RESN 23B4		R8E5 RESN 26B7		U2T1 SC26B6 25D7		
	R6H4 RESN 39B7		R7E5 RESN 24A4		R8E6 RESN 26B7		U3D1 LH55B 49B6 49B6		
	R6H5 RESN 43B5		R7E6 RESN 23D8		R8E7 QWL ISOLATION 26B2		U3B2 FET_VREG 31D5		
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