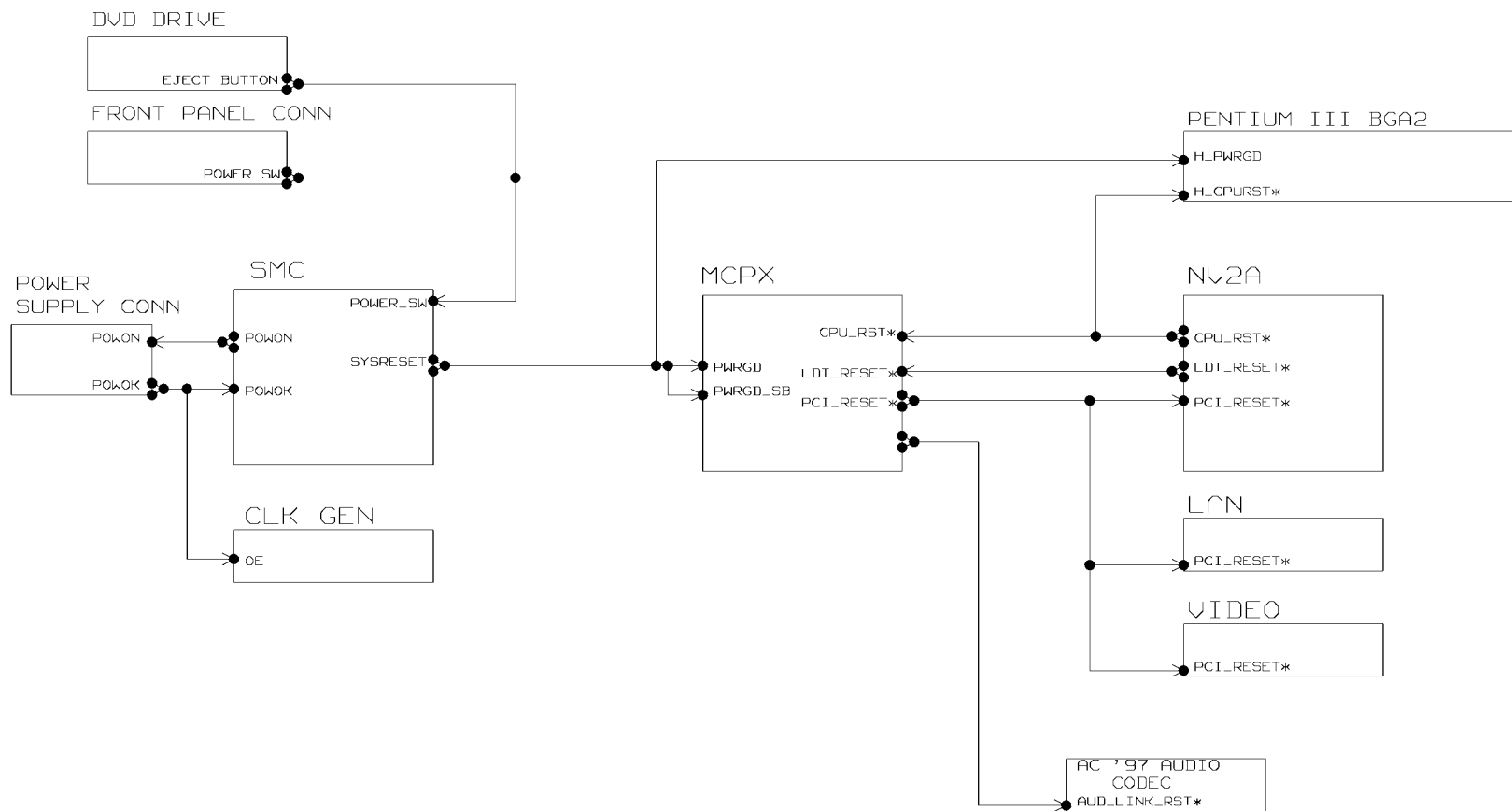


CR-1 8		7		6		5		4		3FULL_ID=1145-1-16118		2PAGE_INFO_ID=16118OWNED_BY=DES		MODULE_ID=532-1-61421DONOR_ID=532-1-6142							
										SCHEMATIC REV 9.0		PBA NUMBER A32646-900		REV 01		BOM RELEASE DATE 08/30/01					
PAGECONTENTS										PAGECONTENTS											
[1]COVER PAGE]										[26]CPU VOLTAGE REGULATOR]											
[2]BLOCK DIAGRAM]										[27]CPU VREG OUTPUT FILTER]											
[3]RESET MAP]										[28]1.5V SWITCHING REGULATOR]											
[4]GPIO/IDSEL TABLE]										[29]CLOCK GENERATOR]											
[5]PENTIUM III BGA2 PART 1 OF 4]										[30]1.25V SWITCHING REGULATOR]											
[6]PENTIUM III BGA2 PART 2 OF 4]										[31]LINEAR_REGULATORS_1.5_2.5]											
[7]PENTIUM III BGA2 PARTS 3 & 4]										[32]DVT POWER CONNECTOR]											
[8]CPU VCORE DECOUPLING]										[33]BULK DECOUPLING]											
[9]CPU VTT DECOUPLING]										[34]SUPERCAP VBAT REGULATOR]											
[10]ITP TERMINATION]										[35]LAN ICS1893]											
[11]NV2A 1 OF 2(NORTH BRIDGE)]										[36]LAN JACK/THERMAL SENSE/EEPROM]											
[12]NV2A 2 OF 2(NORTH BRIDGE)]										[37]IDE]											
[13]NV2A STRAPPING]										[38]AUDIO CODEC]											
[14]DDR SDRAM (PARTITION A)]										[39]AUDIO NO POP]											
[15]DDR SDRAM (PARTITION B)]										[40]AUDIO AMPLIFIER]											
[16]DDR SDRAM (PARTITION C)]										[41]AUDIO VREG AND BIAS]											
[17]DDR SDRAM (PARTITION D)]										[42]VIDEO DAC AND TV ENCODER]											
[18]DDR PARALLEL TERM DATA A/B]										[43]AV CONNECTOR]											
[19]DDR PARALLEL TERM DATA C/D]										[44]LABELS AND MOUNTING HOLES]											
[20]VTERM DECOUPLING]										[45]FLASH]											
[21]MEMORY DECOUPLING]										[46]USB FRONT PANEL]											
[22]NV2A DECOUPLING]										[47]NV2A FAN/5V DRAIN/BROWN OUT]											
[23]MCPX 1 OF 2]										[48]SMC/FAN/DVD PWR/FRONT PANEL]											
[24]MCPX 2 OF 2]										[49]MCPX MUXED PIN ASSIGNMENT]											
[25]MCPX INPUT STRAPS]										[50-55]INDEX]											
NOTES:																					
1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.																					
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.																					
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.																					
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.																					
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.																					
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.																					
[PAGE_TITLE=COVER PAGE]										DRAWING DUTFABK.SCH.1.1 Thu Aug 30 08:43:02 2001											
[DONOR_REV=1.0/999999] [DONOR_PROJ=DVT_A--532]										[PROJ_REV=4.0/999999] [PROJ_NAME=DVT_D--1145] [MODULE=NONE]6											
										5											
										4											
										LAST_MAKEPROJ: 4/12/01 1:13:37 PM3											
										2											
										1											
										BOM RELEASE DATE XX/XX/XX						PB NUMBER A38727-009					
										SIGNATURE						DATE					
										DRN BY						intel3855 BOWERS AVE SANTA CLARA, CA 95051					
										CHK BY XX000X						XX/XX/XX					
										ENGR APVD						TITLE SCH, PBA, DVT					
										APVD						INTEL					
										APVD						CONFIDENTIAL					
																DOCUMENT NUMBER A72507					
																PAGE 1\55					
																REV 9.0					

RESET & POWER-ON MAP

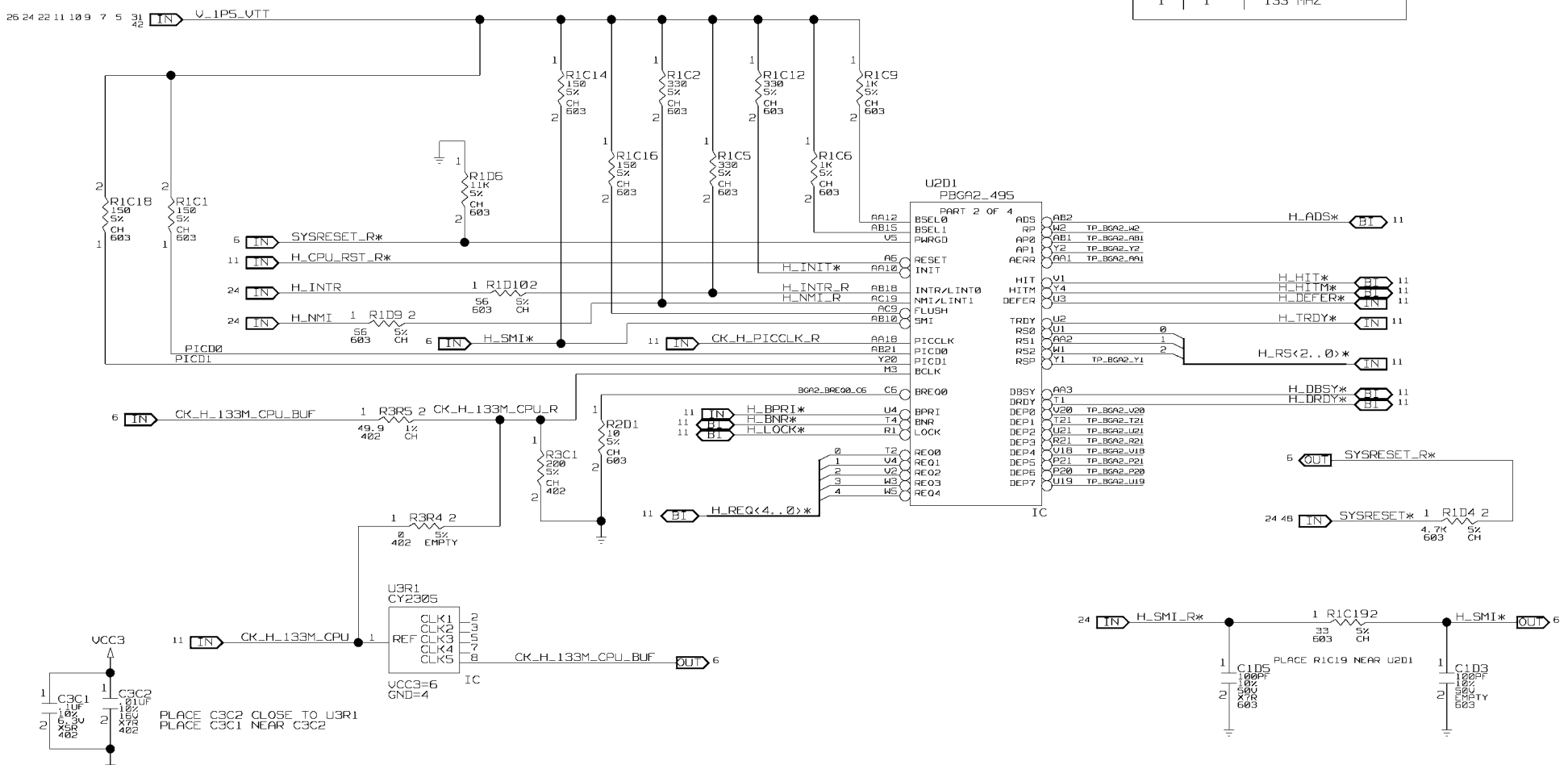


[PAGE_TITLE=RESET MAP]

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DUTFABK. SCH. 1:3
Thu Aug 30 08:40:21 2001

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	3	3.0

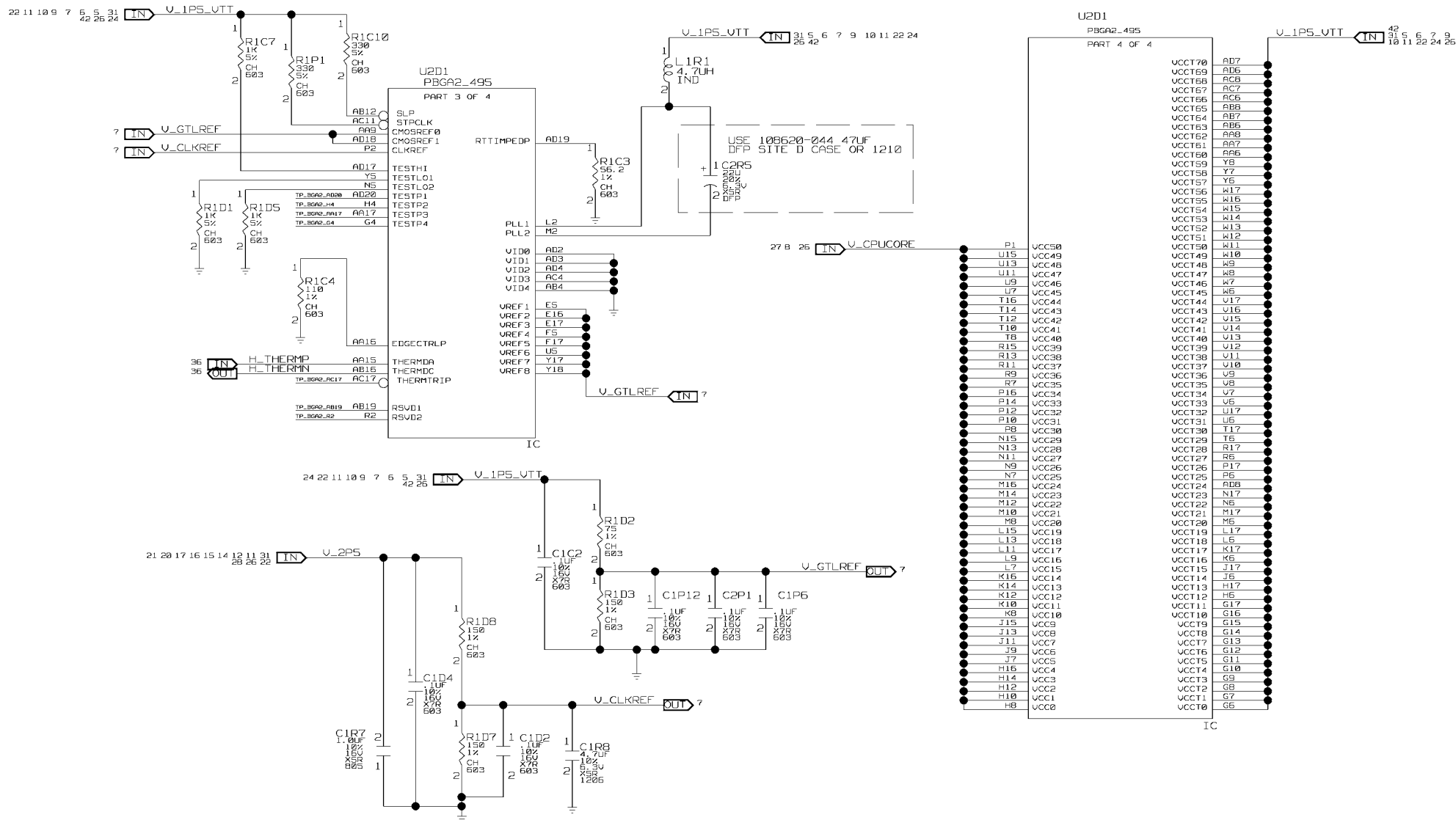
BSEL1	BSEL0	SYSTEM BUS FREQUENCY
0	0	RESERVED
0	1	100 MHz
1	0	RESERVED
1	1	133 MHz



[PAGE_TITLE=PENTIUM III BGA2 PART 2 OF 4]

DRAWING
DUTFABK. SCH. 1.6
Thu Aug 30 08:40:30 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER A72507	PAGE 6	REV 9.0
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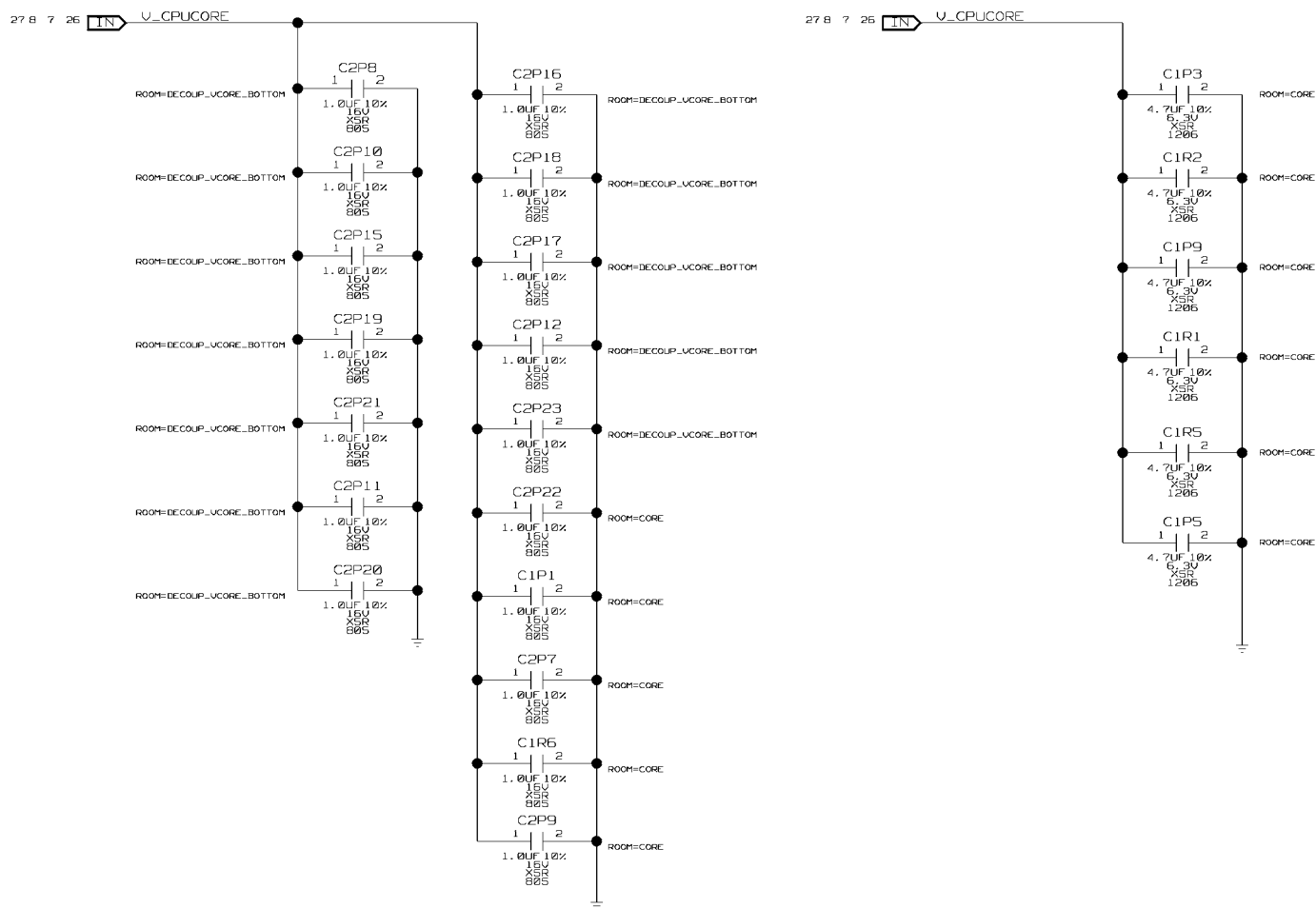


[PAGE_TITLE=PENTIUM III BGA2 PARTS 3 & 4]

DRAWING
DUTFABK, SCH. 1.7
Thu Aug 30 08:40:33 2001

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	7	3.0

CPU VCORE DECOUPLING

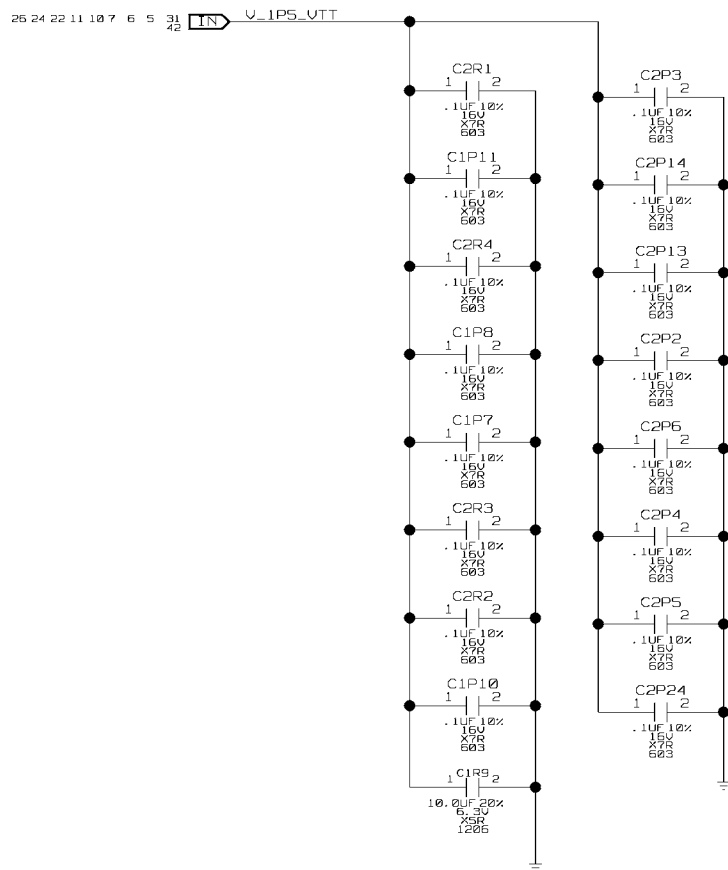


[PAGE_TITLE=CPU VCORE DECOUPLING]

DRAWING
DUTFABK SCH. 1:8
Thu Aug 30 08:40:35 2001

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	8	3.0

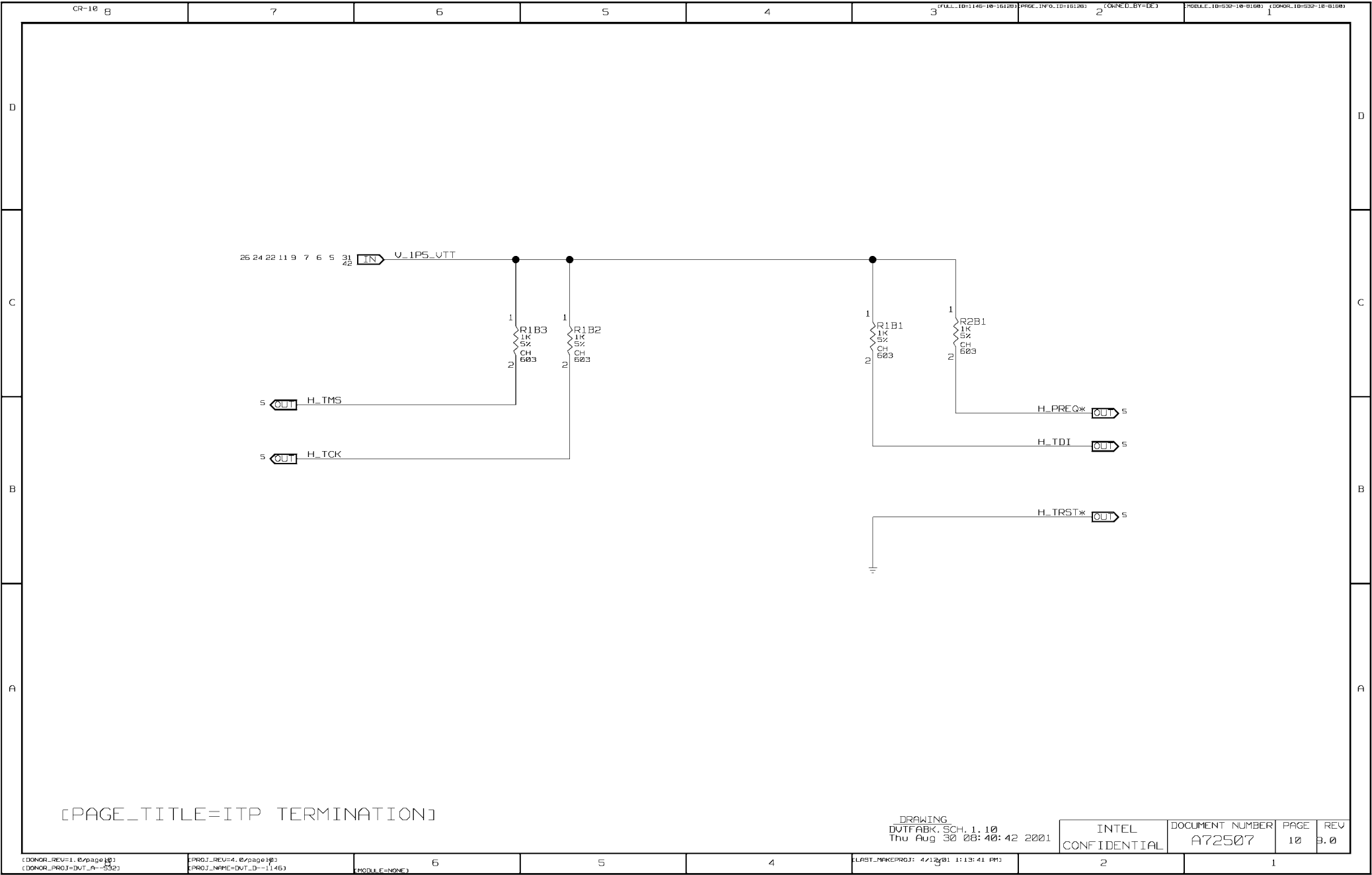
CPU VTT DECOUPLING

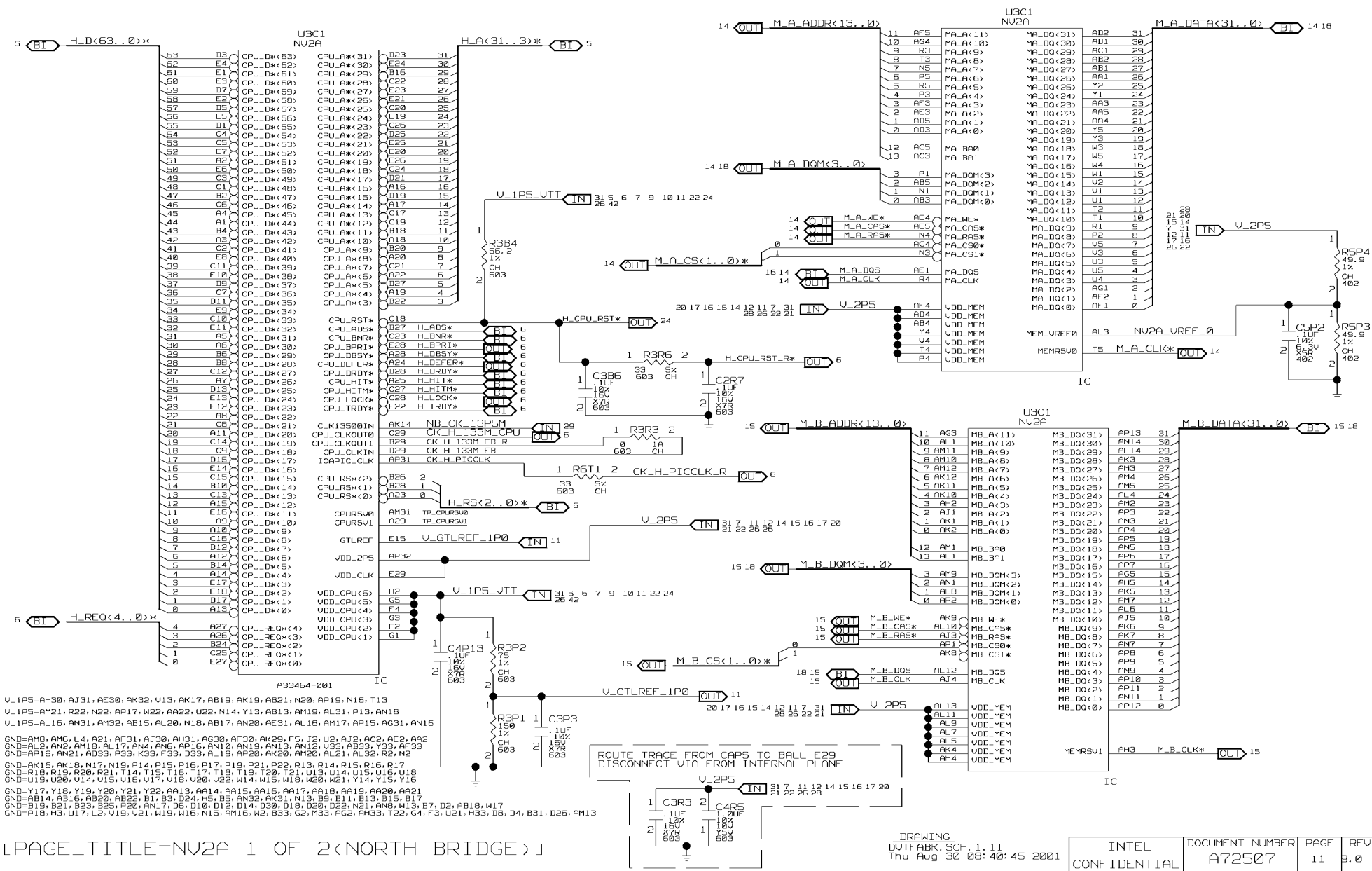


[PAGE_TITLE=CPU VTT DECOUPLING]

DRAWING
DUTFABK. SCH. 1:9
Thu Aug 30 08:40:39 2001

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	9	3.0



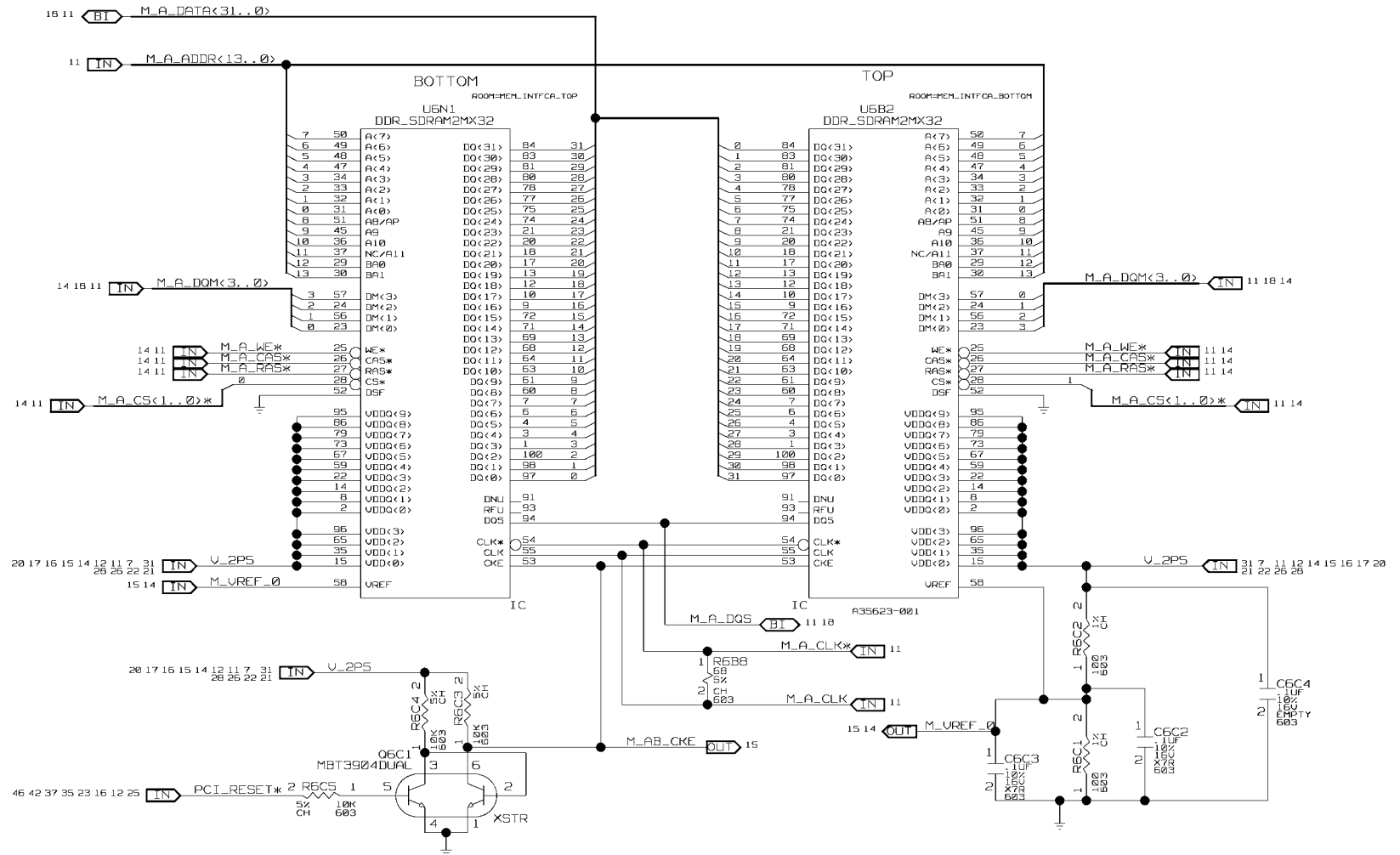


[PAGE_TITLE=NV2A 1 OF 2(NORTH BRIDGE)]

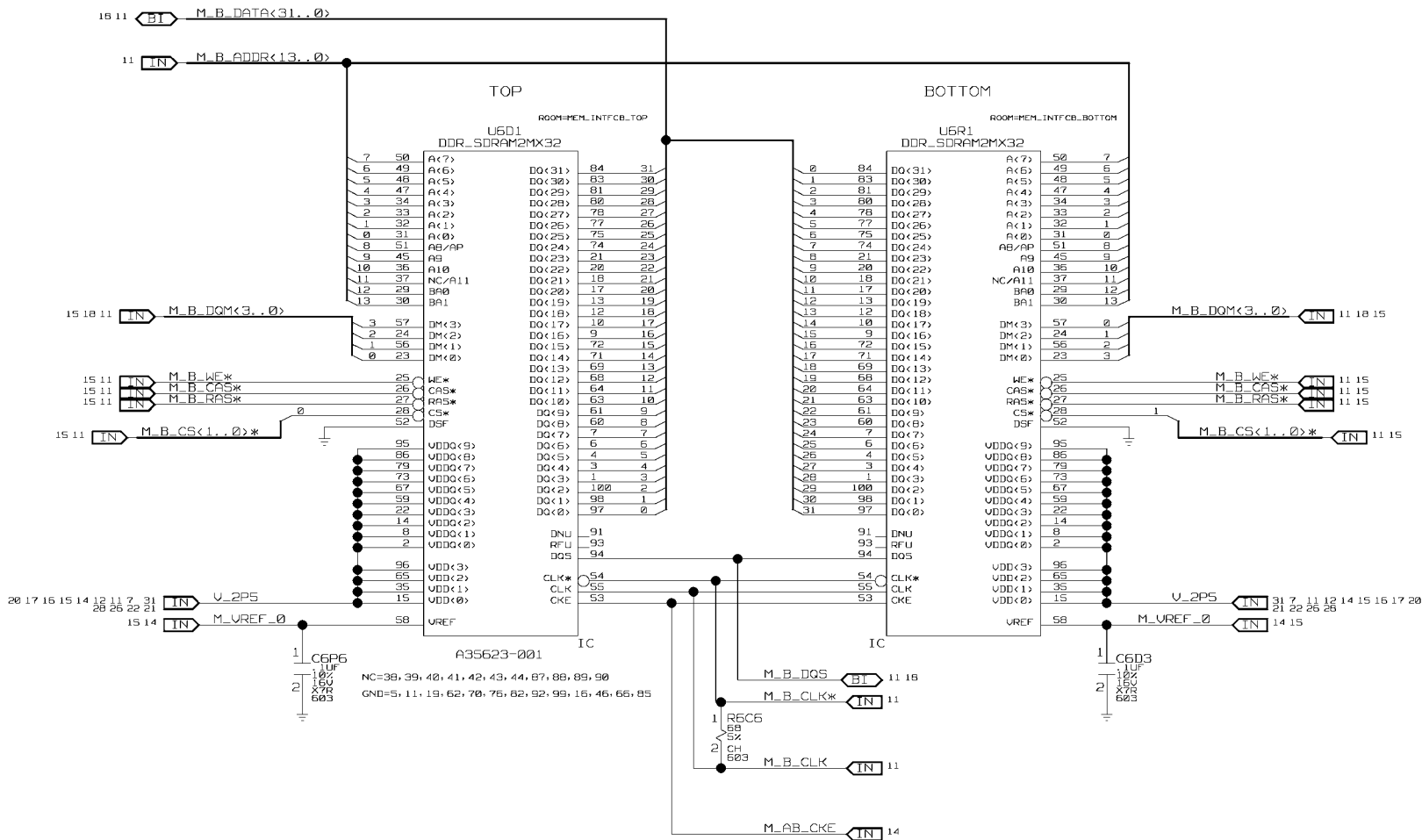
DRAWING
DUTFABK. SCH. 1. 11
Thu Aug 30 08:40:45 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER A72507	PAGE 11	REV 3.0
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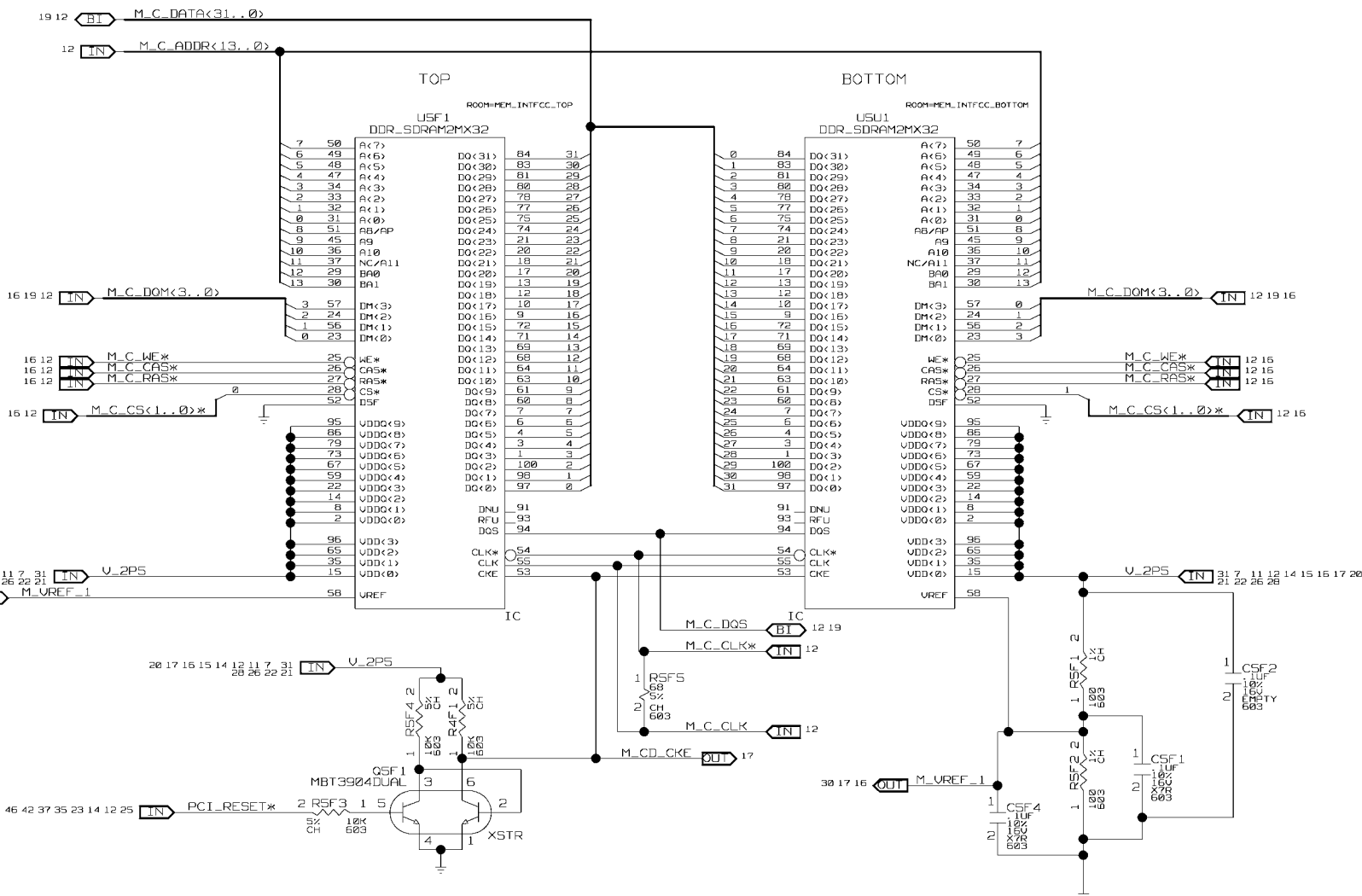
MEMORY INTERFACE PARTITION A



MEMORY INTERFACE PARTITION B



MEMORY INTERFACE PARTITION C

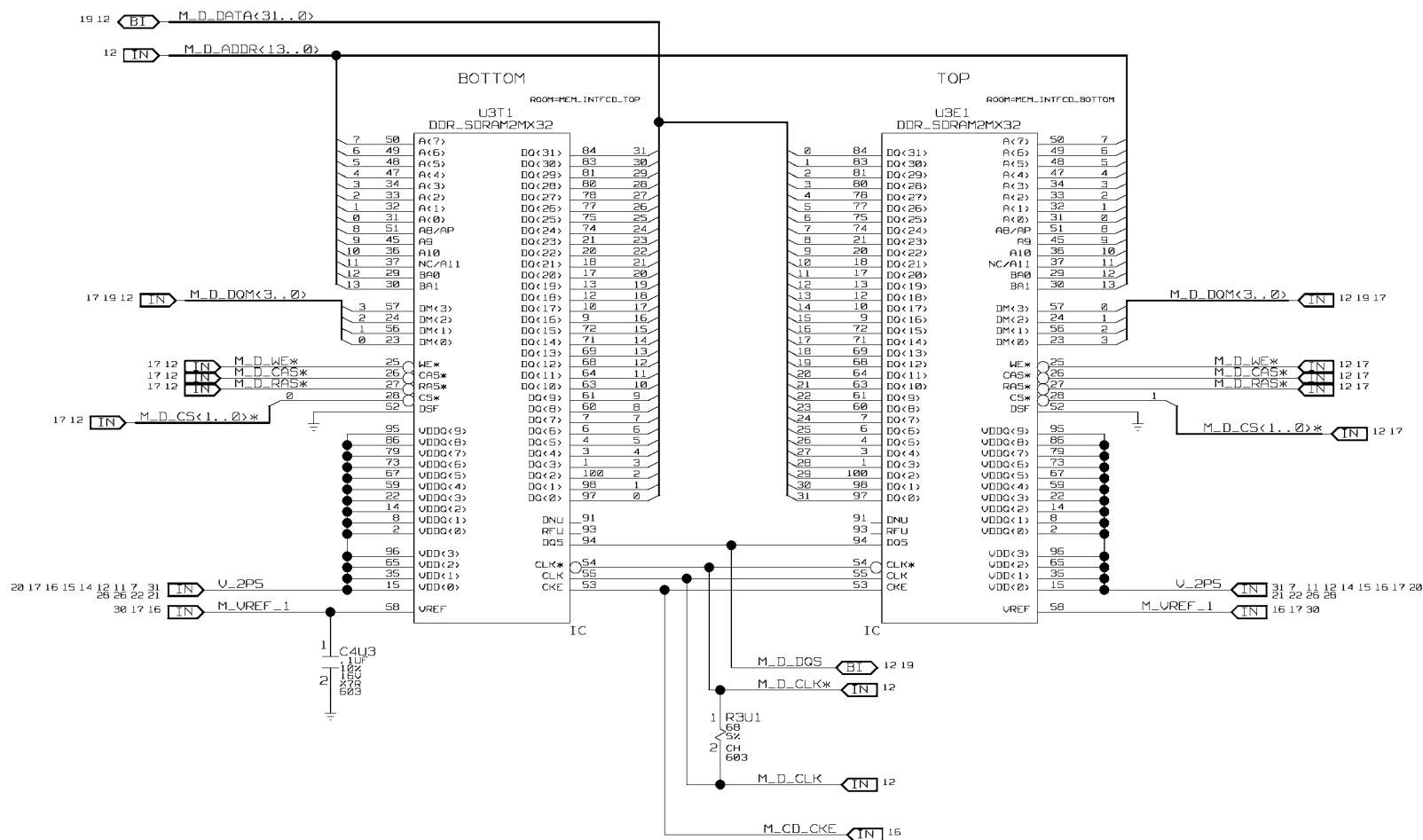


[PAGE_TITLE=DDR SDRAM (PARTITION C)]

DRAWING
DUTFABK SCH. 1: 16
Thu Aug 30 08:41:01 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER A72507	PAGE 16	REV 3.0
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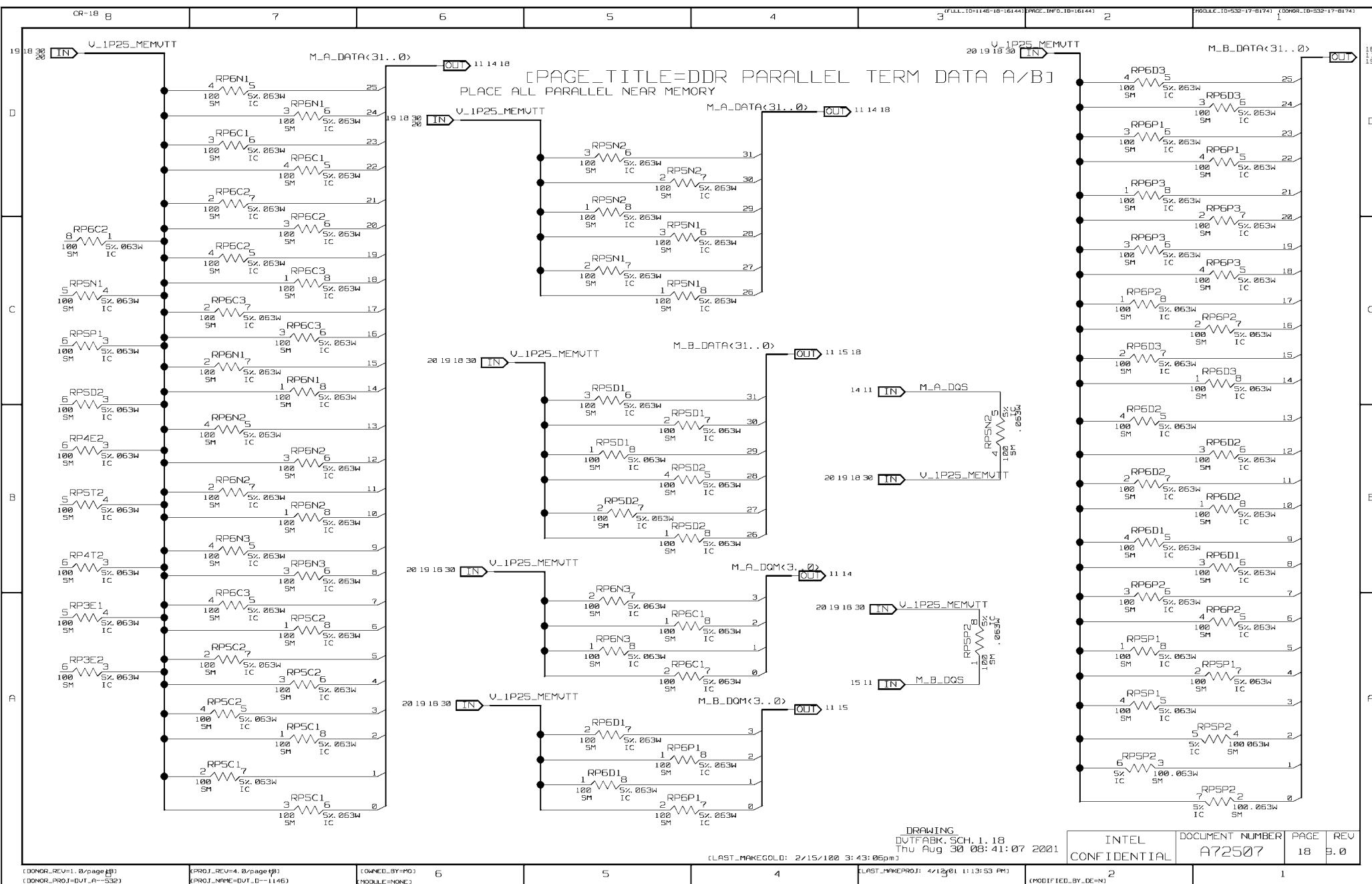
MEMORY INTERFACE PARTITION D

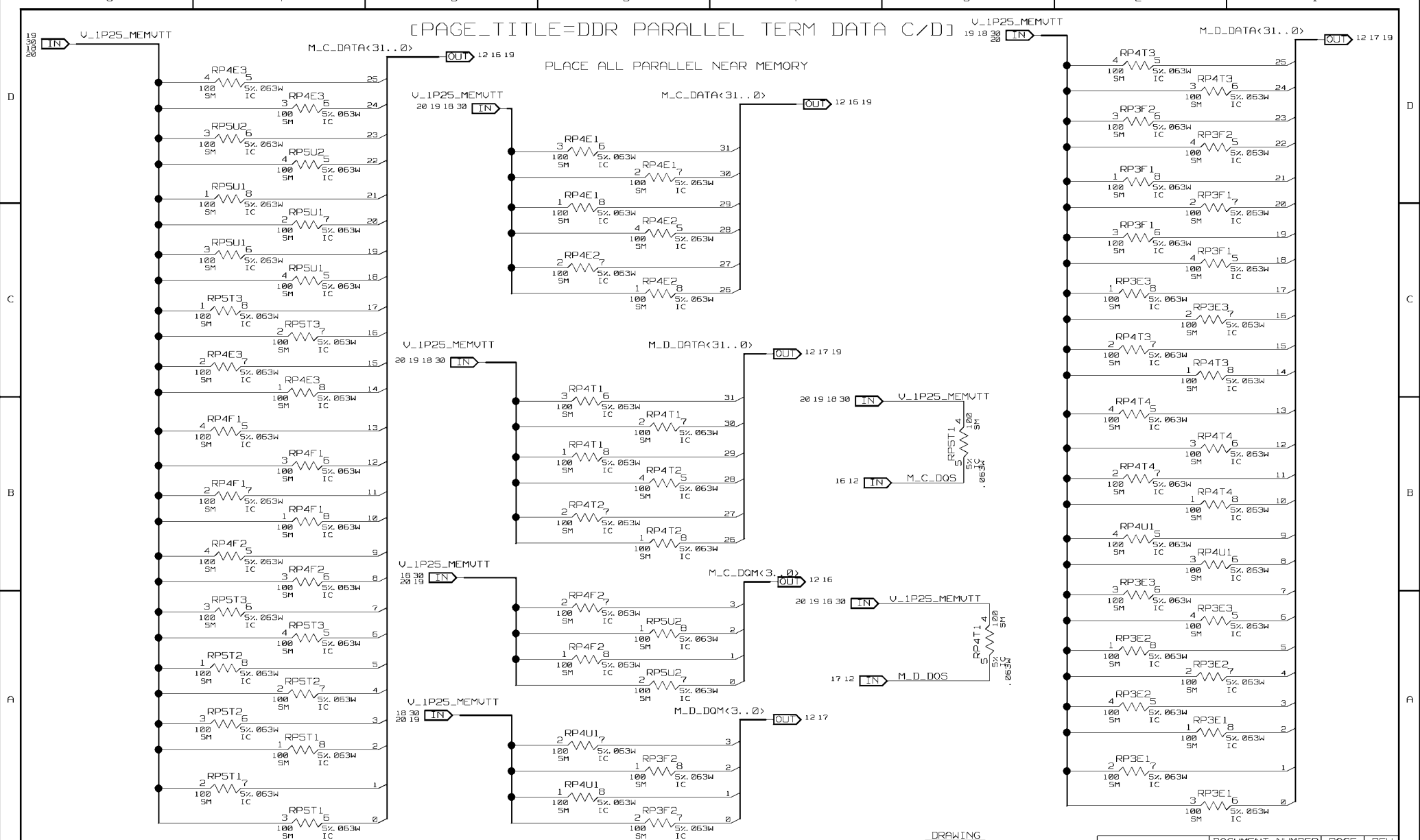


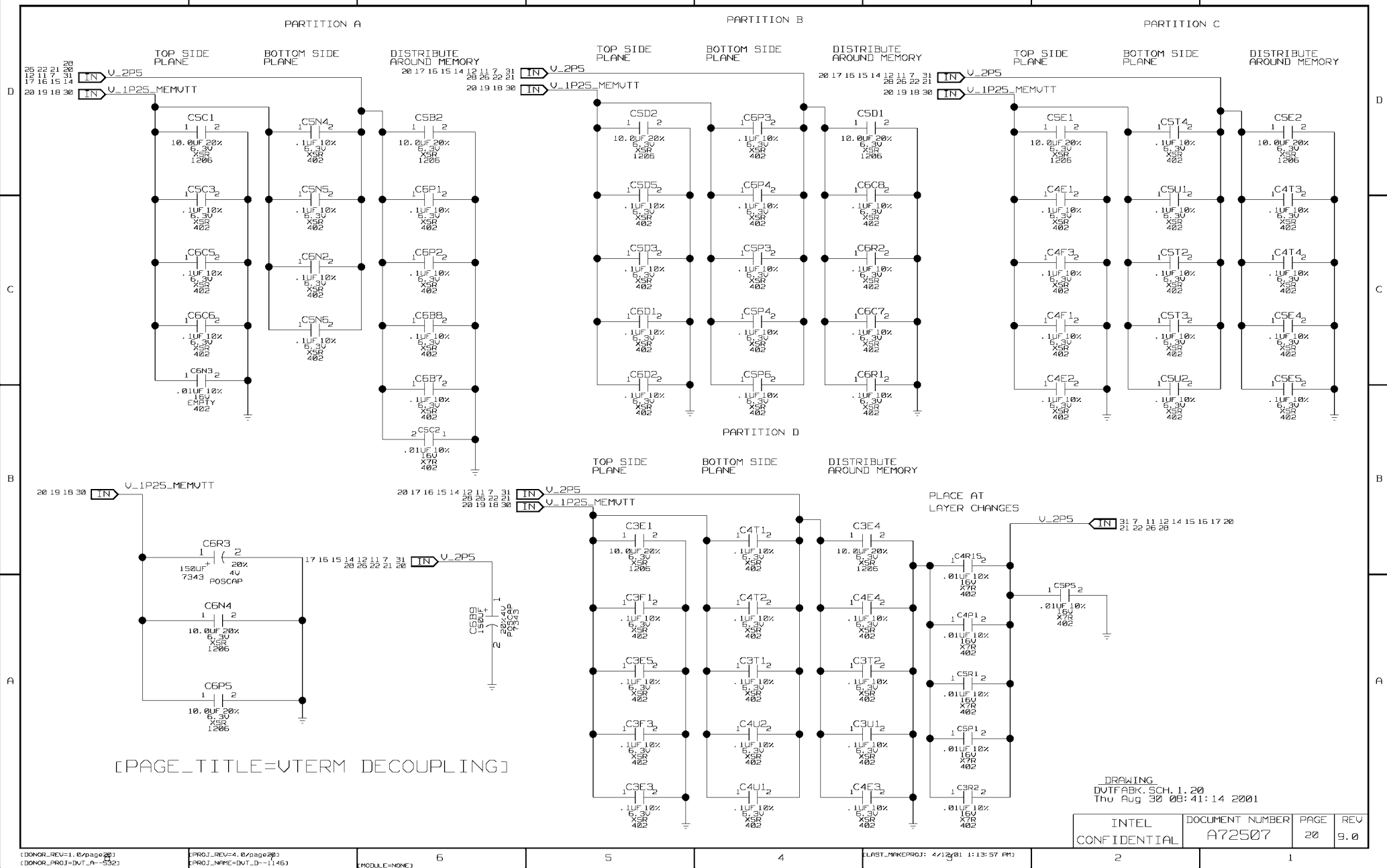
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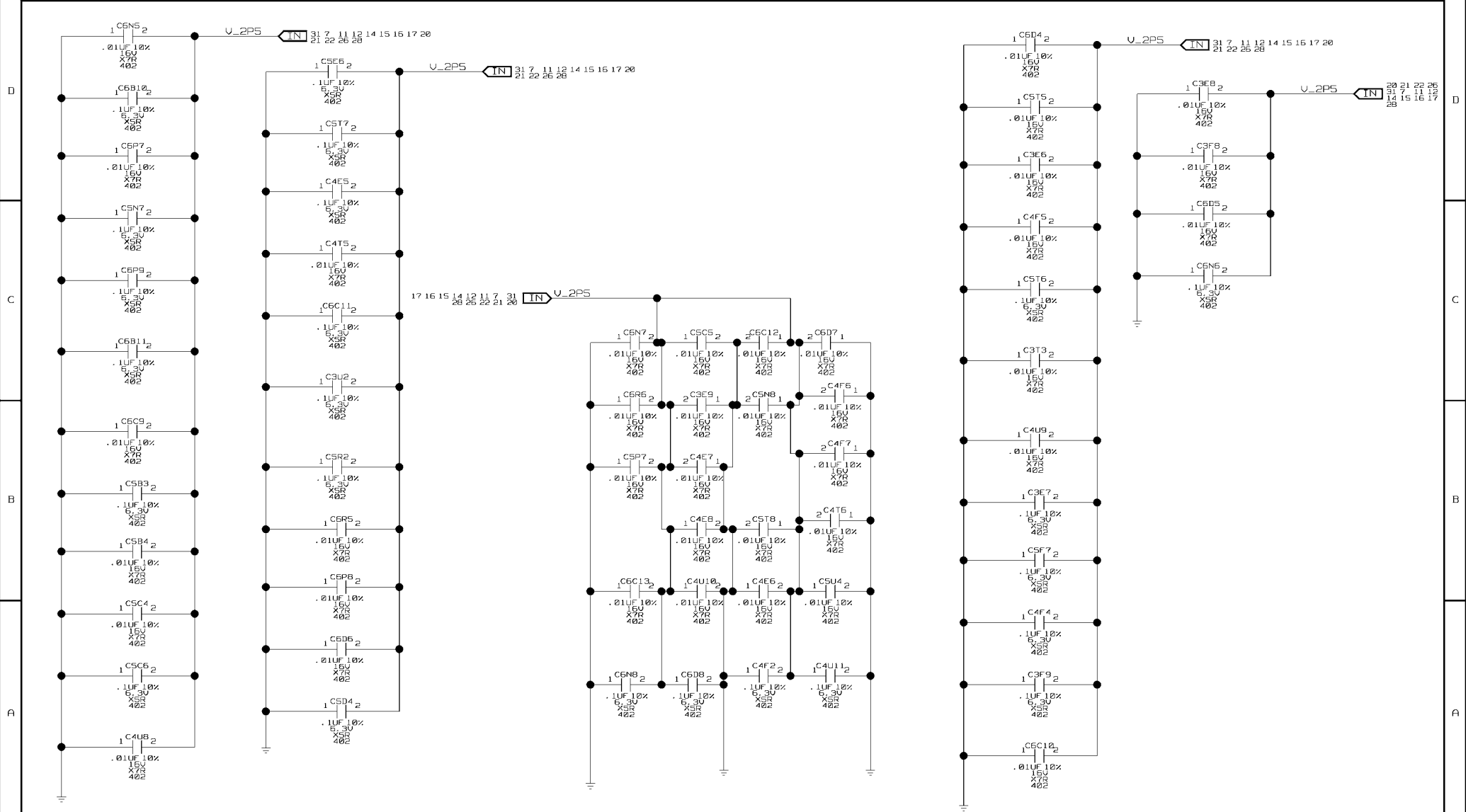
DRAWING
DUTFABK, SCH. 1: 17
Thu Aug 30 08:41:04 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER A72507	PAGE 17	REV 3.0
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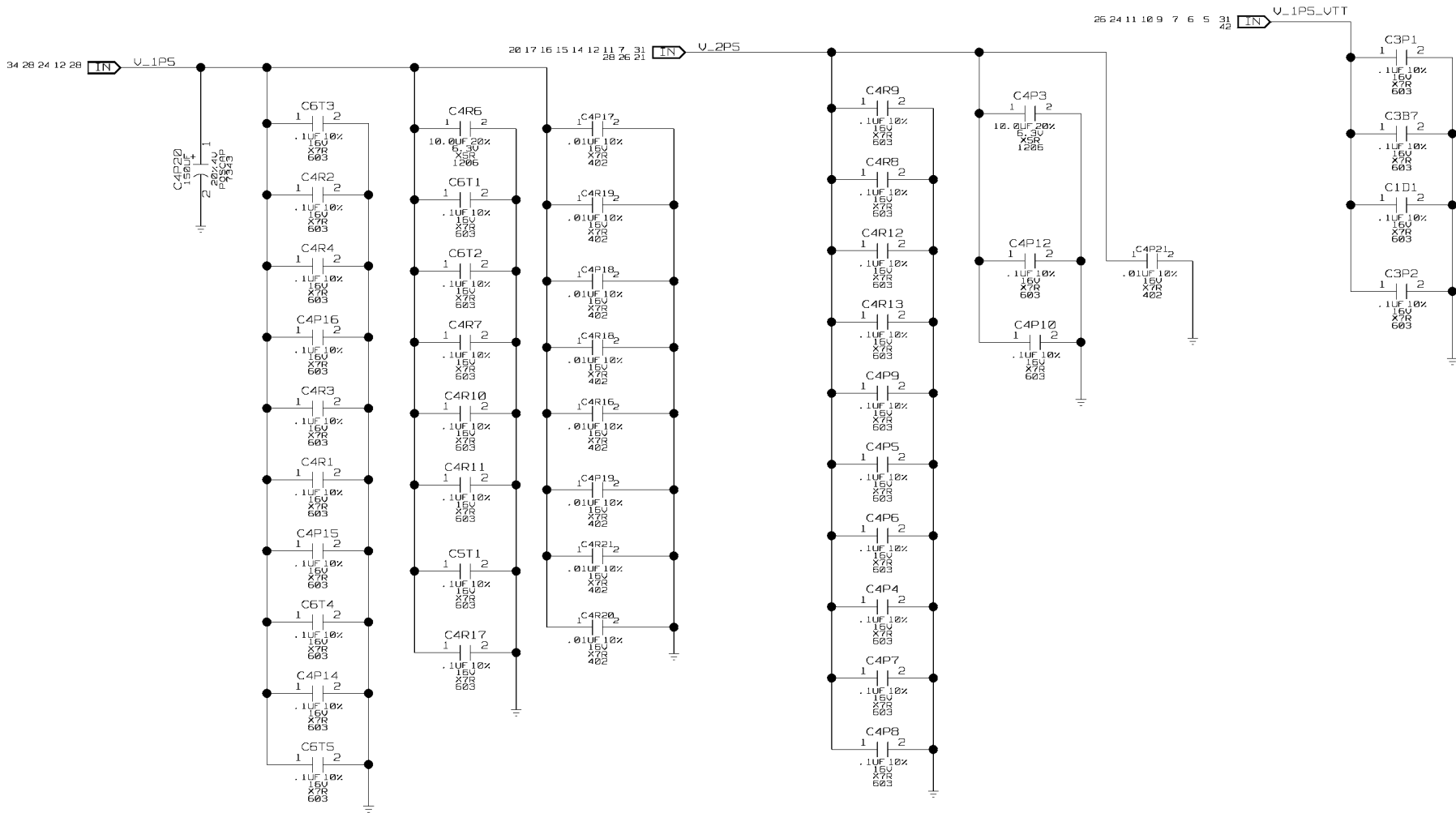






[PAGE_TITLE=MEMORY DECOUPLING]

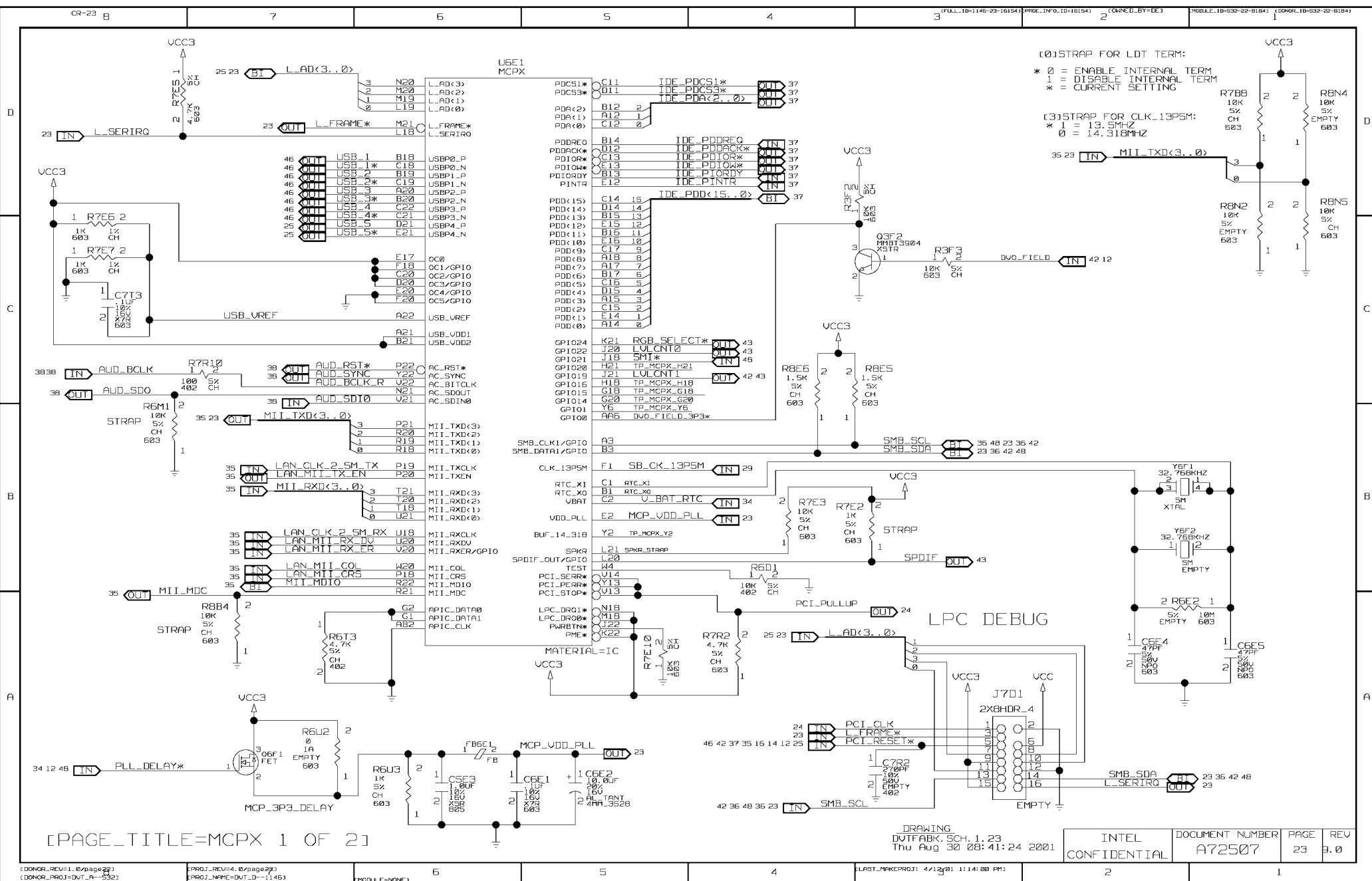
NV2A DECOUPLING

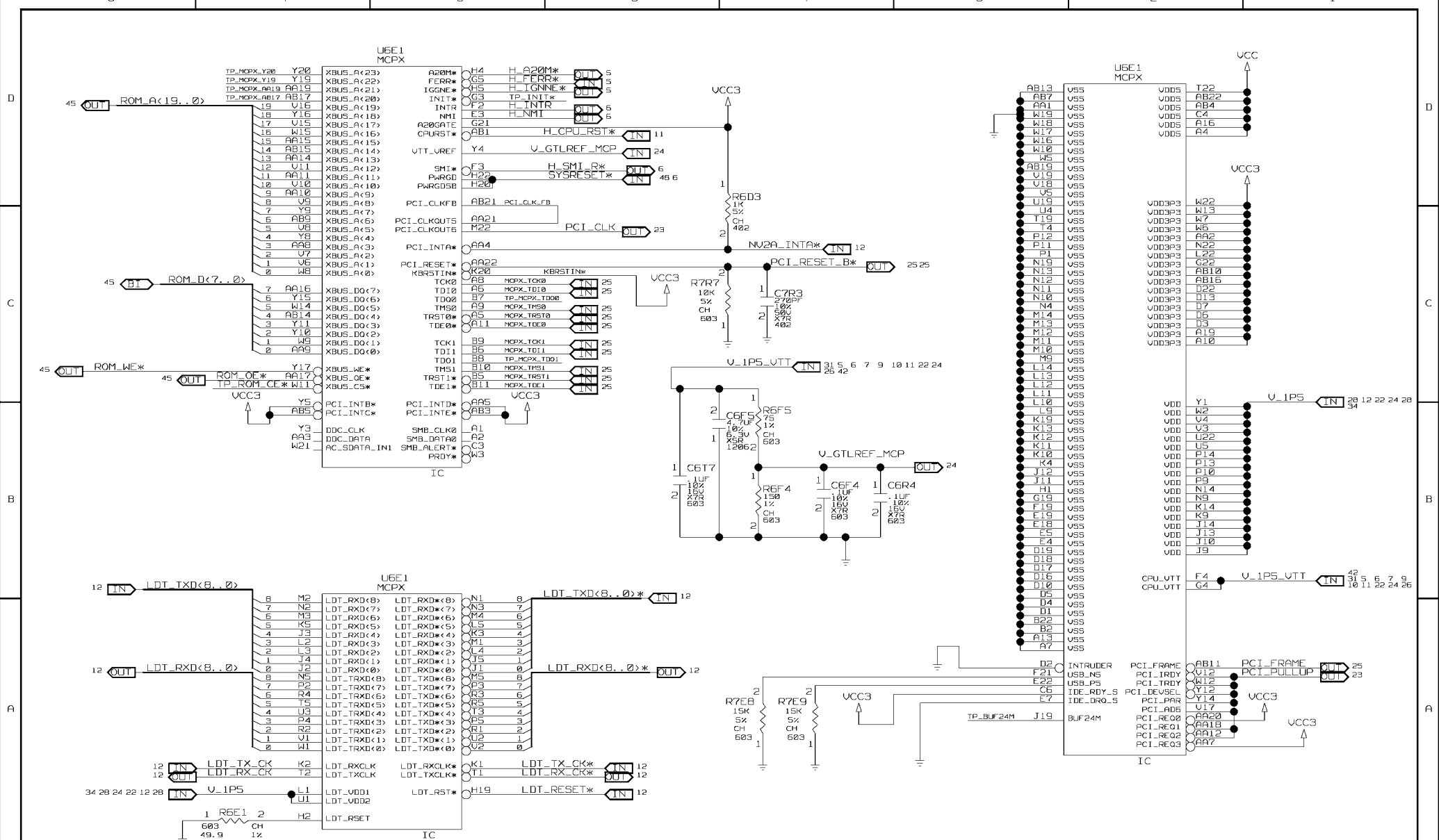


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DRAWING
DUTFABK. SCH. 1: 22
Thu Aug 30 08:41:20 2001

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	22	9.0

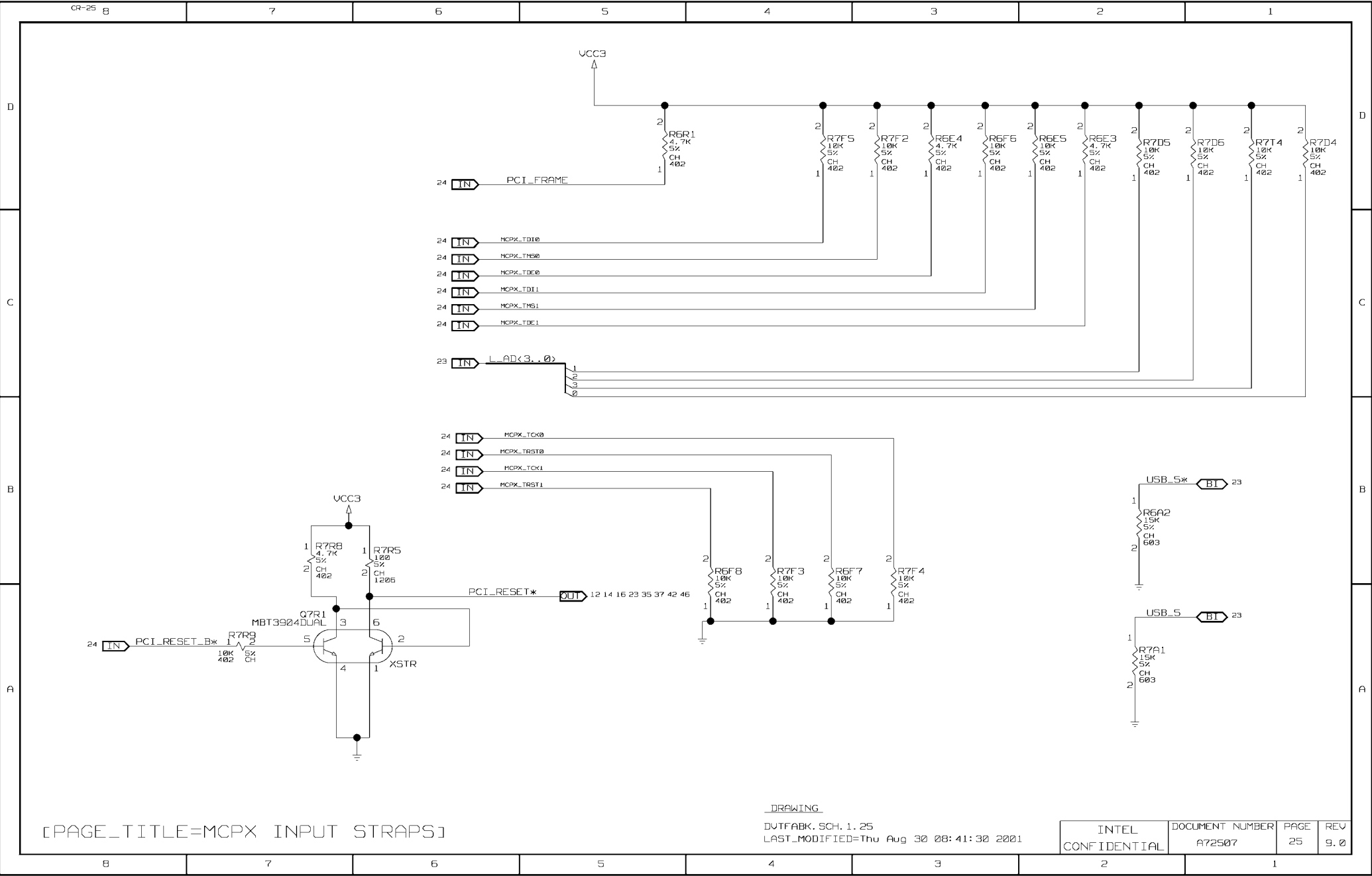


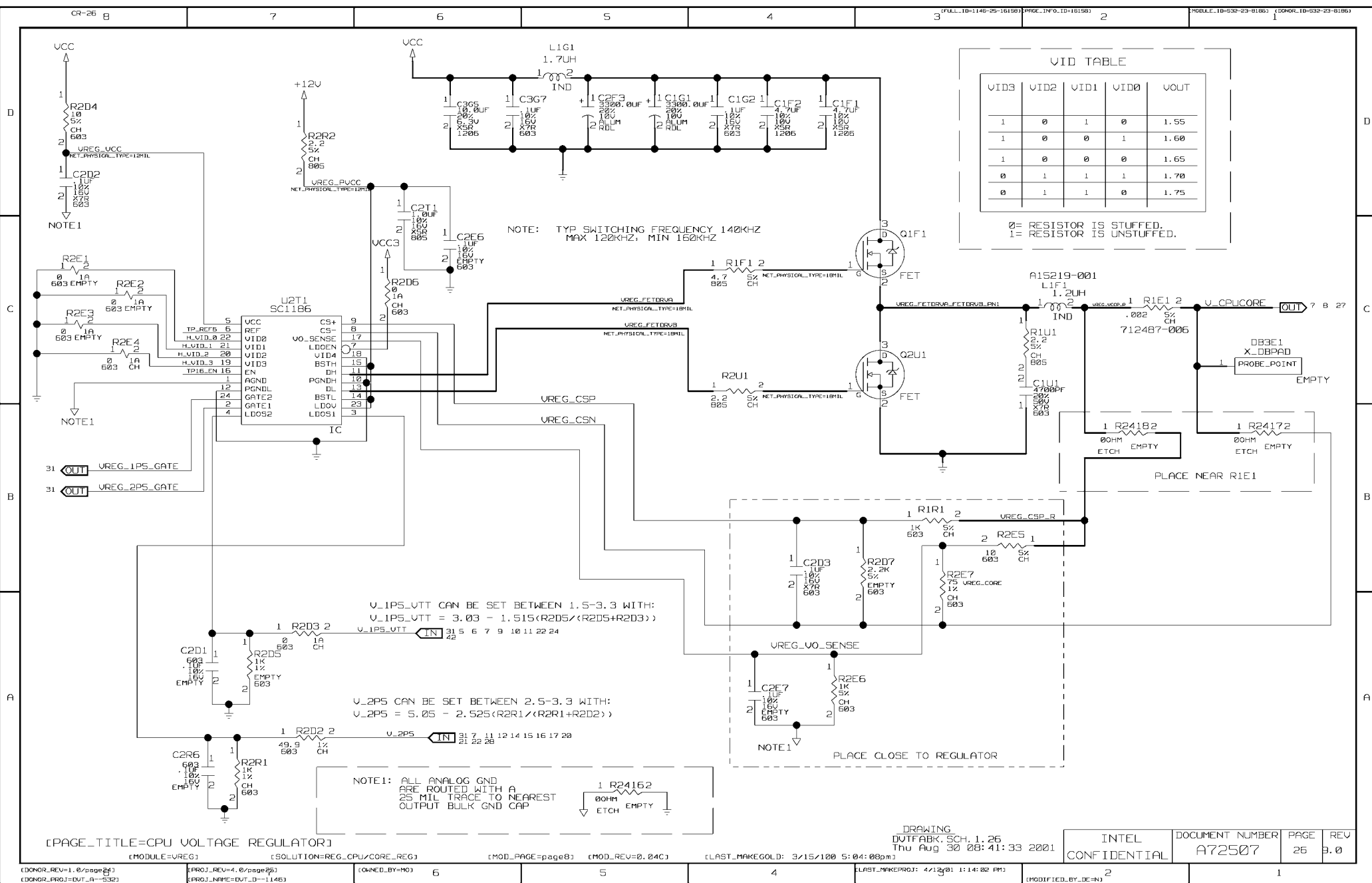


[PAGE_TITLE=MCPX 2 OF 2]

DRAWING
DUTFABK, SCH. 1.24
Thu Aug 30 08:41:27 2001

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	24	9.0







D

C

B

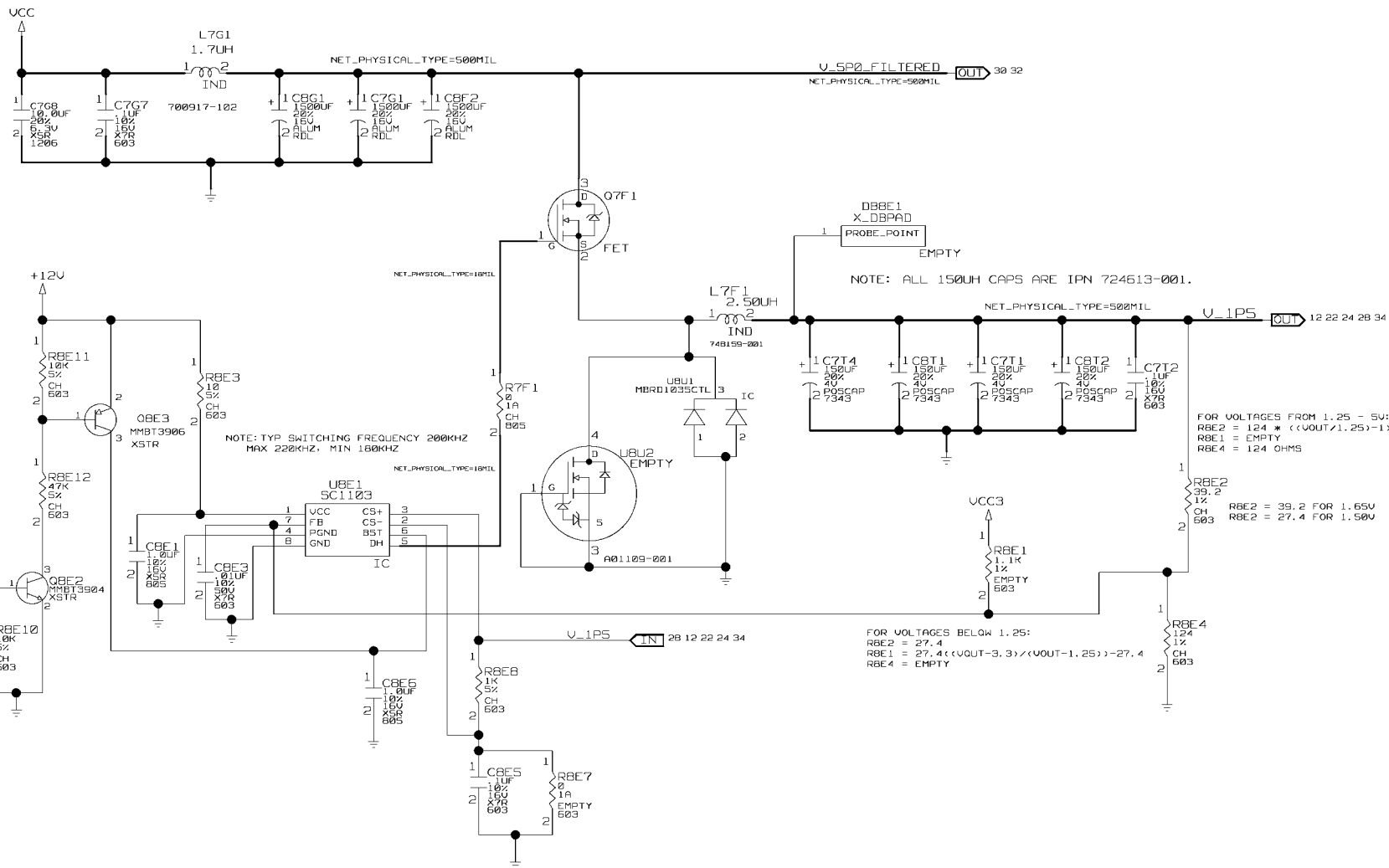
A

D

C

B

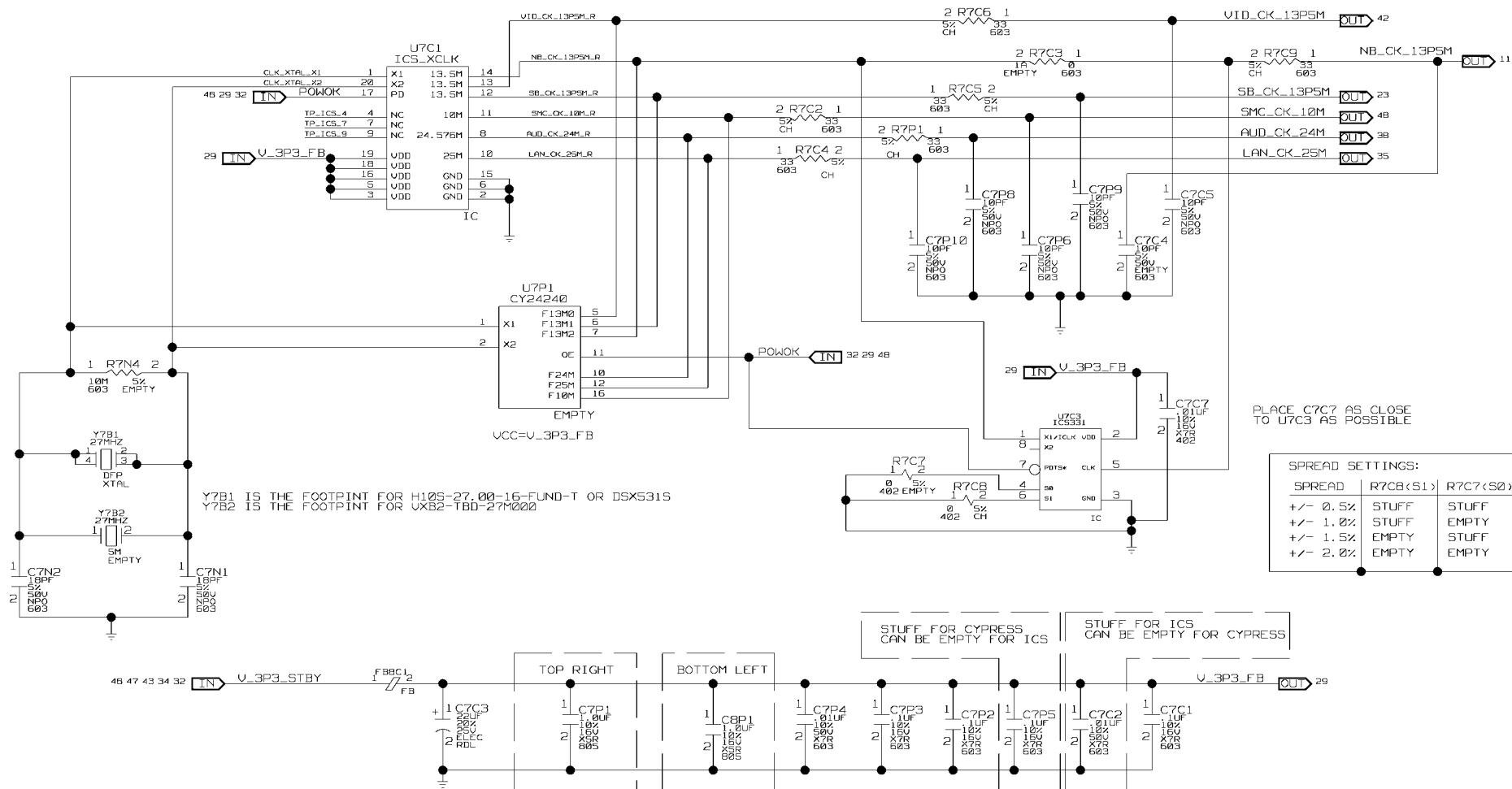
A



[PAGE_TITLE=1.5V SWITCHING REGULATOR]

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Thu Aug 30 08:41:39 2001

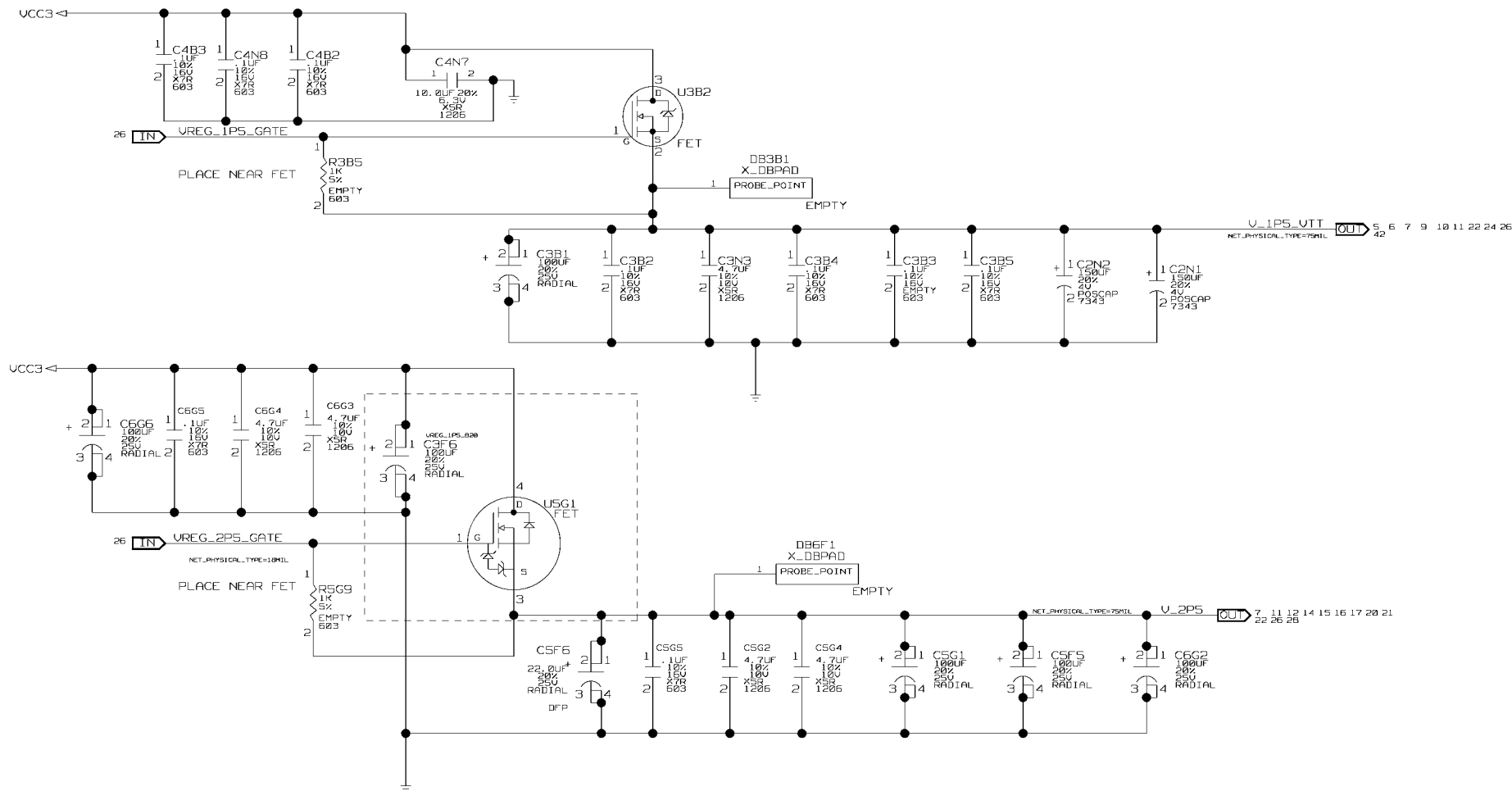
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	28	3.0



[PAGE_TITLE=CLOCK GENERATOR]

DRAWING
DUTFABK, SCH. 1: 29
Thu Aug 30 08:41:42 2001

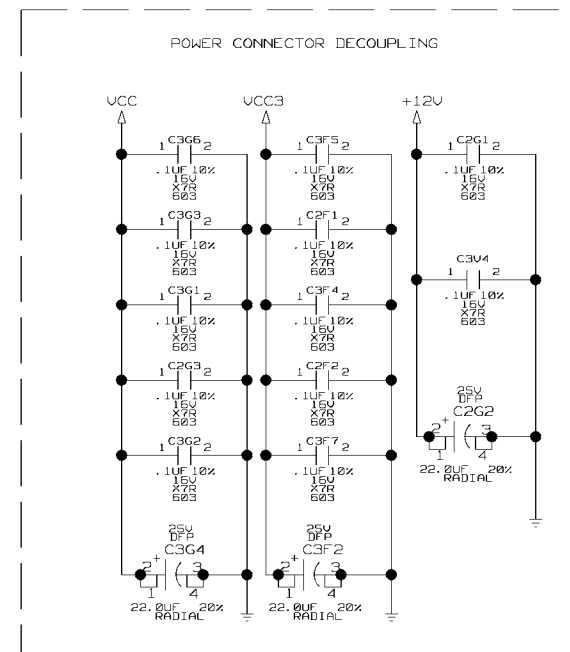
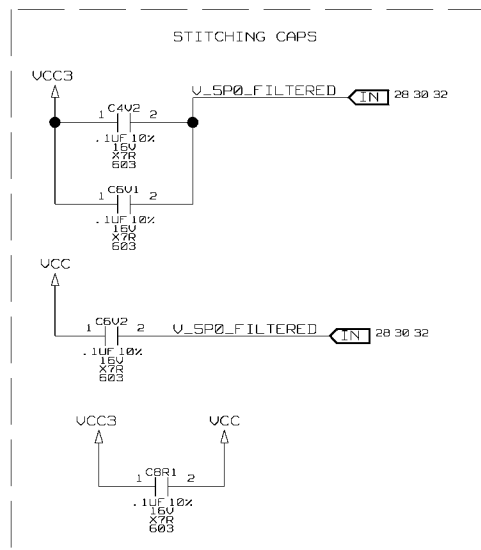
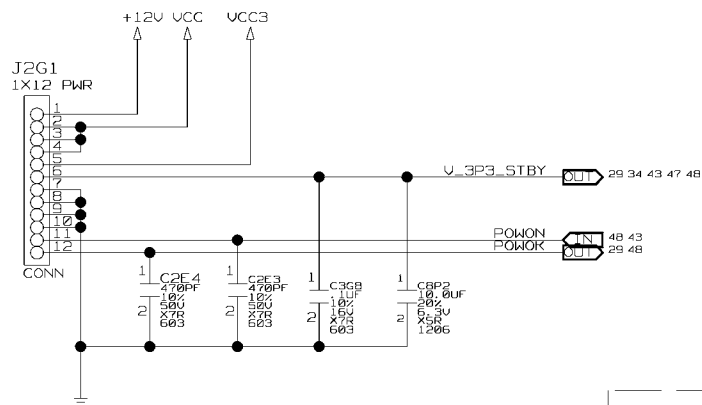
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CONFIDENTIAL	A72507	29	3.0



[PAGE_TITLE=LINEAR_REGULATORS_1.5_2.5]

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Thu Aug 30 08:41:48 2001

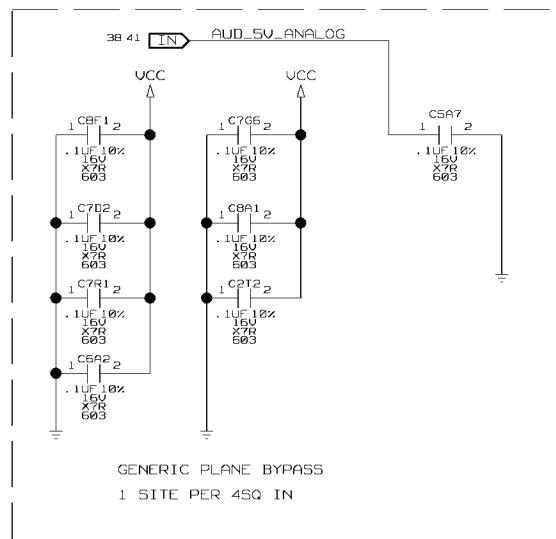
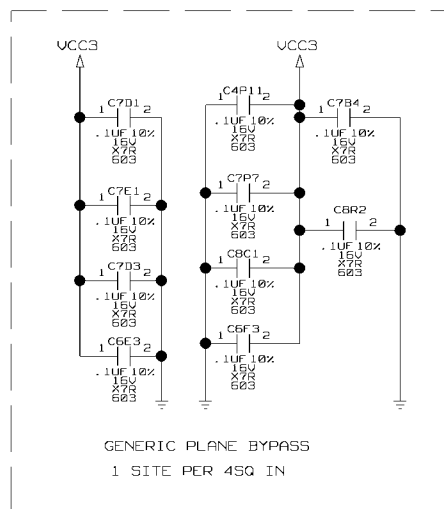
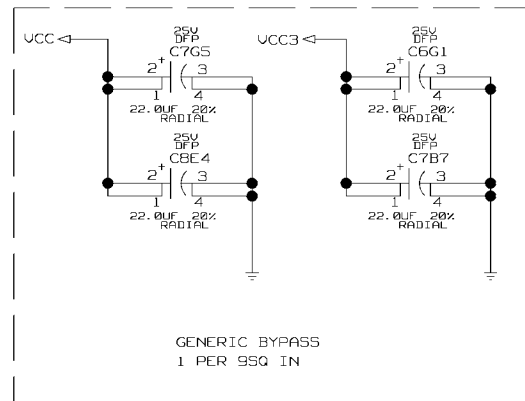
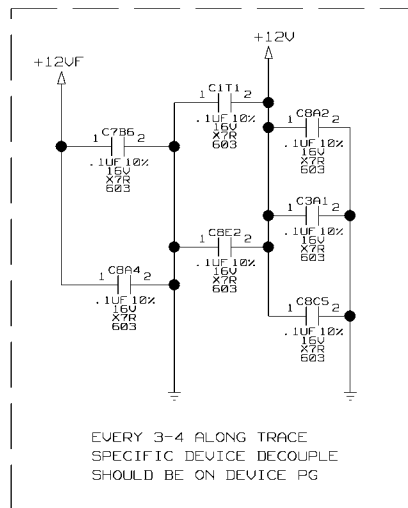
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	31	3.0



[PAGE_TITLE=DVT POWER CONNECTOR]

DRAWING
DUTFABK SCH. 1: 32
Thu Aug 30 08:41:51 2001

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	32	3.0

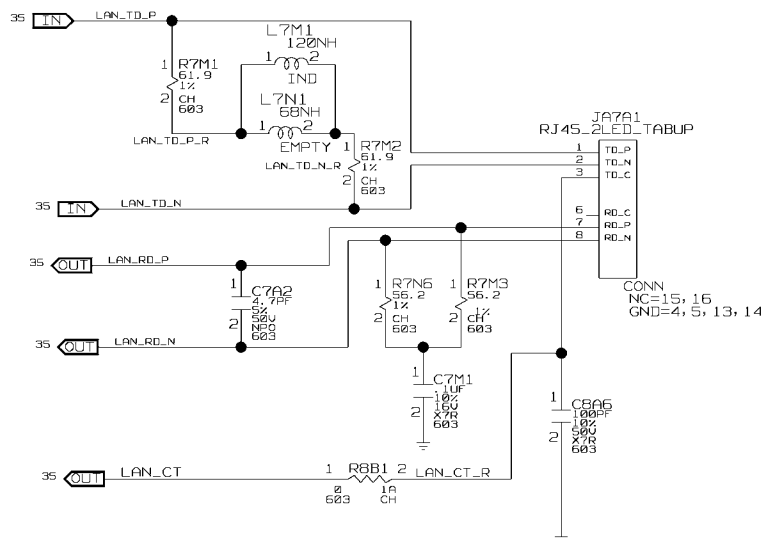


[PAGE_TITLE=BULK DECOUPLING]

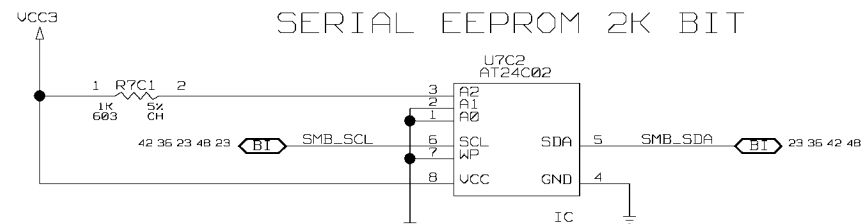
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DUTFABK, SCH. 1: 33
Thu Aug 30 20:41:54 2001

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	33	3.0

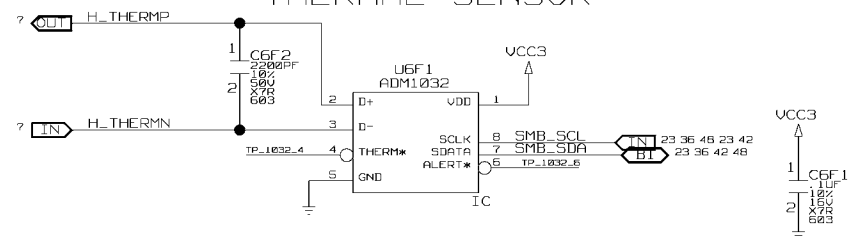
RJ45 SP JACK



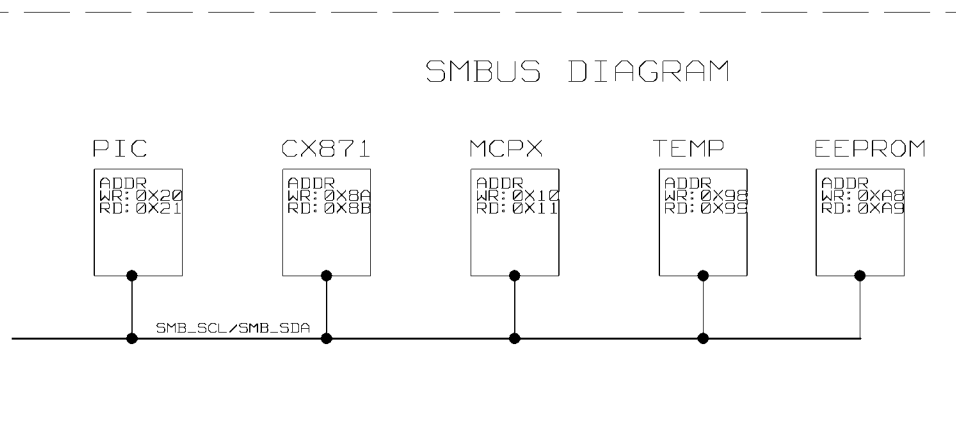
SERIAL EEPROM 2K BIT



THERMAL SENSOR



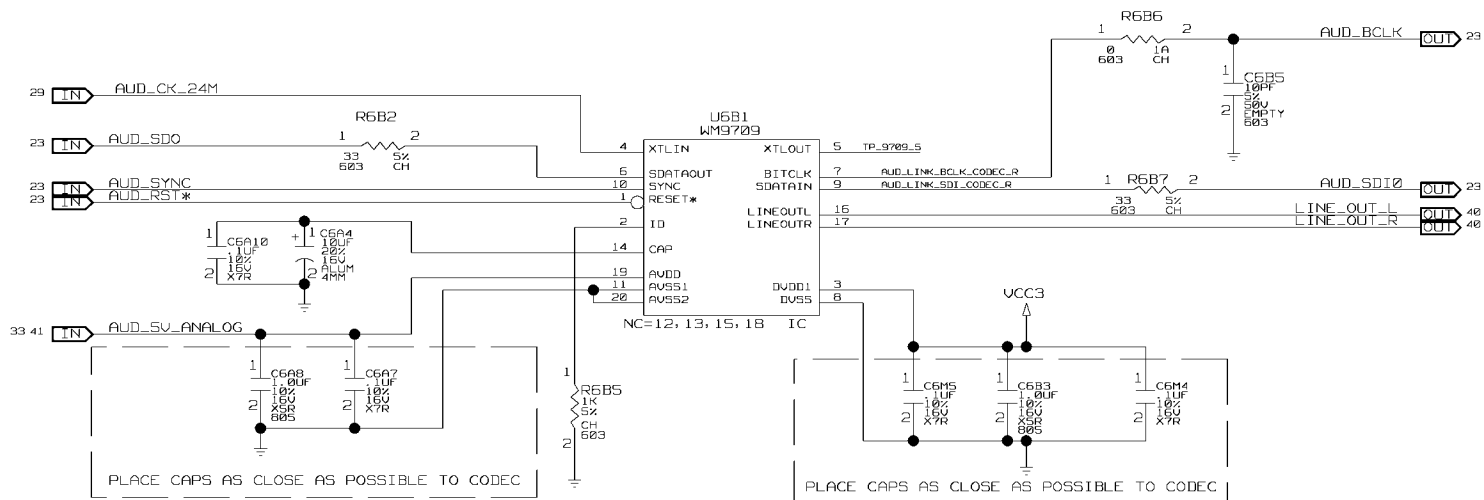
SMBUS DIAGRAM



[PAGE_TITLE=LAN JACK/THERMAL SENSE/EEPROM]

DRAWING
DUTFABK. SCH. 1: 36
Thu Aug 30 08:42:02 2001

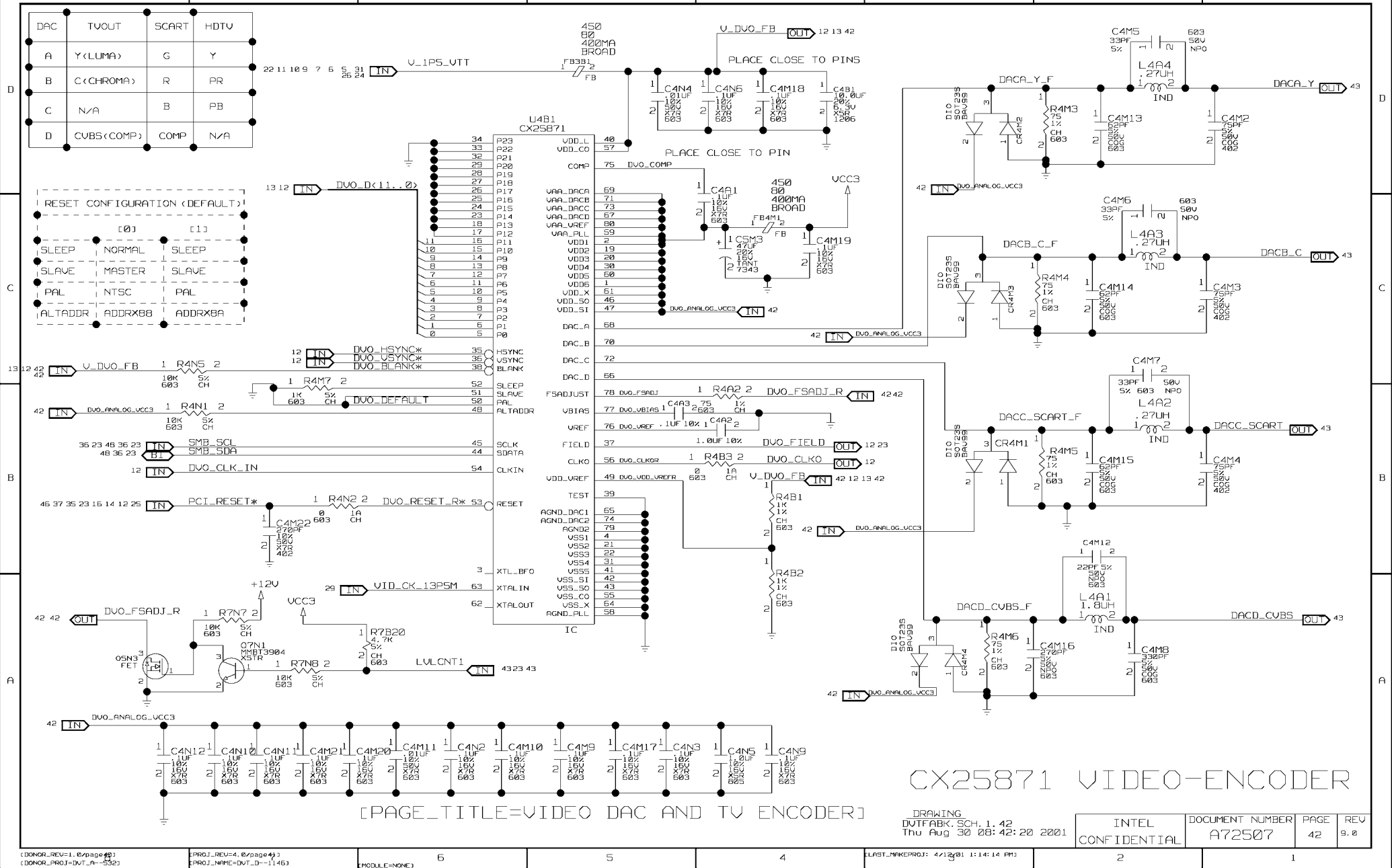
INTEL CONFIDENTIAL	DOCUMENT NUMBER A72507	PAGE 36	REV 3.0
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[PAGE_TITLE=AUDIO CODEC]

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DUTFABK, SCH. 1:38
Thu Aug 30 08:42:08 2001

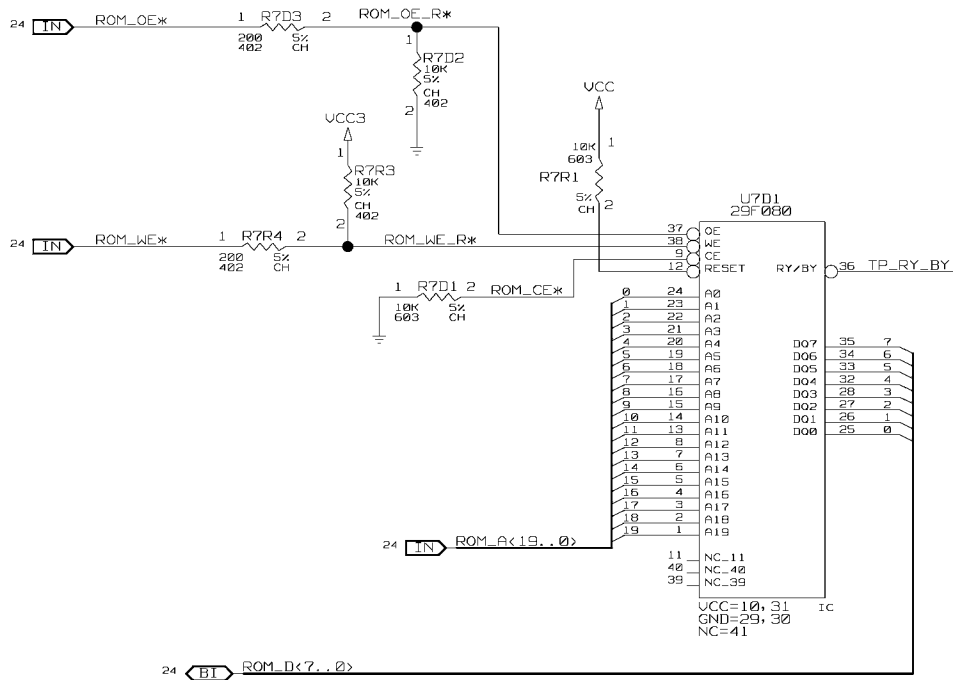
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	38	3.0



[PAGE_TITLE=VIDEO DAC AND TV ENCODER]

CX25871 VIDEO-ENCODER

FOR PRODUCTION:
EMPTY R7D3 AND R7R4

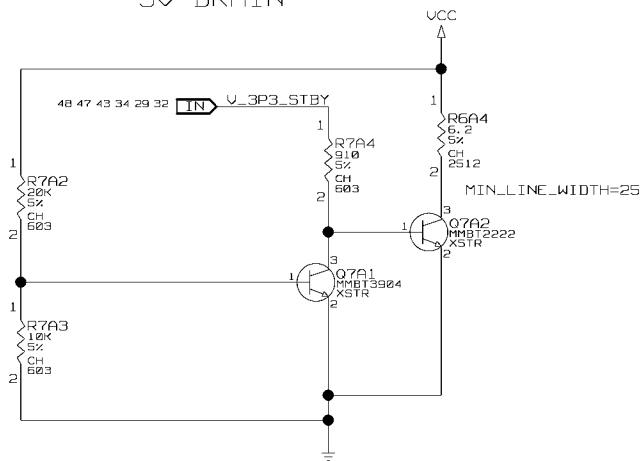


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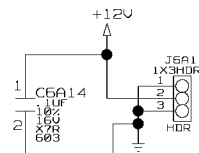
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DUTFABK SCH. 1: 45
Thu Aug 30 08:42:30 2001

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	45	9.0

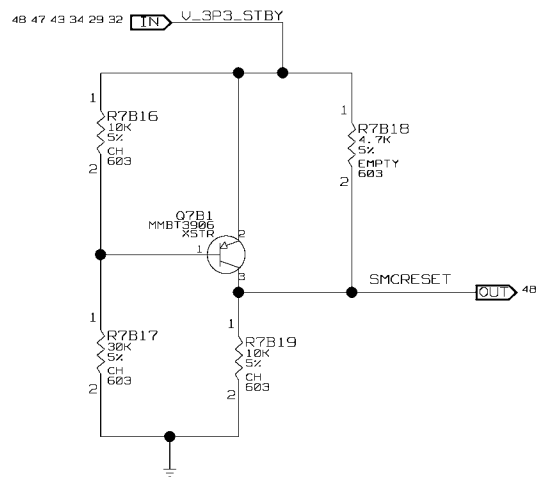
5V DRAIN



NV2A FAN HEADER



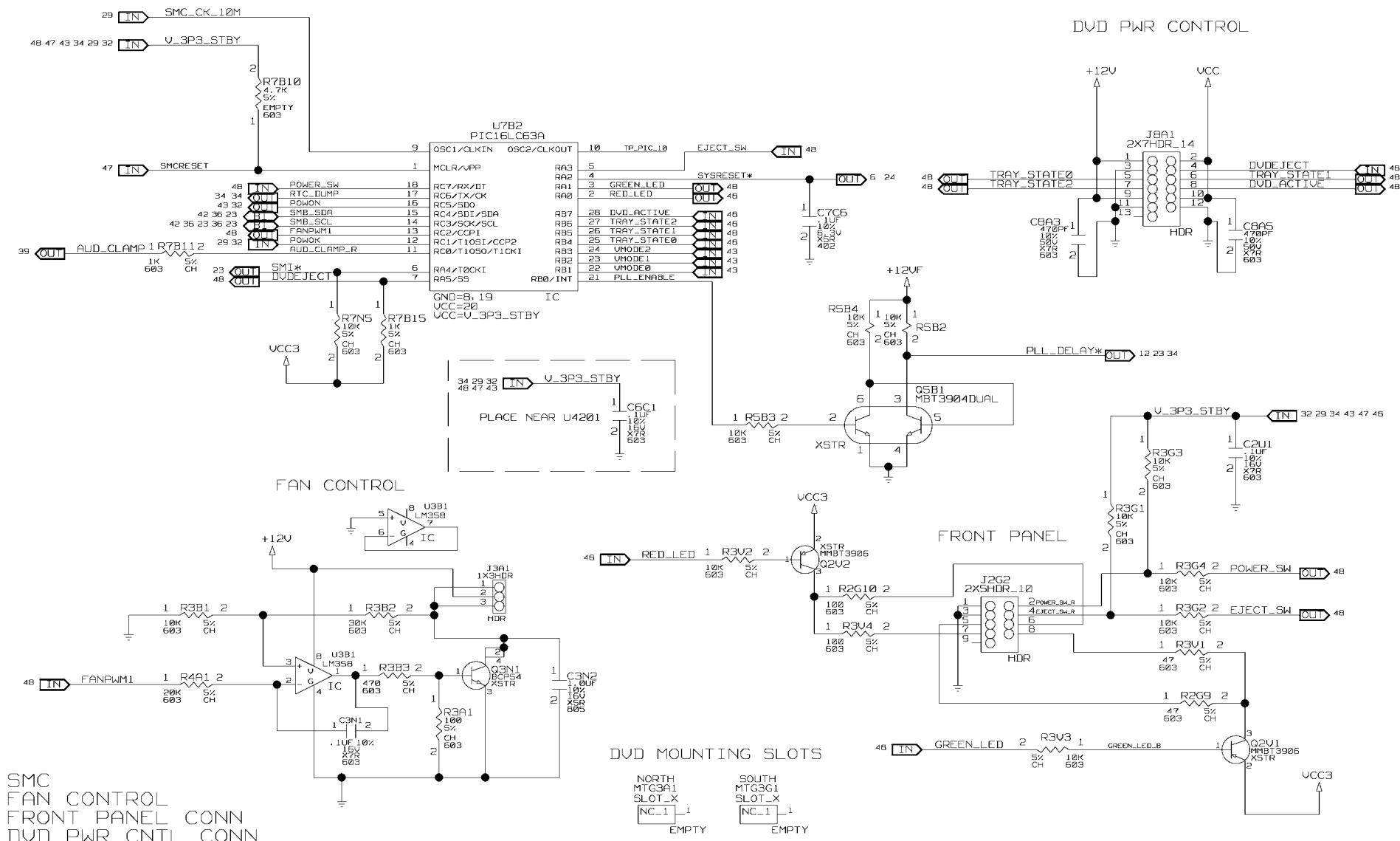
SMC BROWN OUT



[PAGE_TITLE=NV2A FAN/5V DRAIN/BROWN OUT]

DRAWING
DUTFABK, SCH. 1: 47
Thu Aug 30 08:42:35 2001

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	47	3.0



[PAGE_TITLE=SMC/FAN/DVD PWR/FRONT PANEL]

DRAWING
DUTFABK, SCH. 1: 48
Thu Aug 30 08:42:39 2001

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	A72507	48	3.0

MCPX MUXED PIN ASSIGNMENT

BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME	BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME
A5	IDE_ADDR_S0	TRST0	Y20	PCI_AD0	XBUS_A23
E6	IDE_ADDR_S1	RESERVED	Y19	PCI_AD1	XBUS_A22
B5	IDE_ADDR_S2	TRST1	AA19	PCI_AD2	XBUS_A21
C5	IDE_CS1_S*	RESERVED	AB17	PCI_AD3	XBUS_A20
B4	IDE_CS3_S*	RESERVED	AA17	PCI_AD4	XBUS_0E*
A6	IDE_DACK_S*	TDI0	Y17	PCI_AD5	XBUS_WE*
B8	IDE_DATA_S0	TD01	V17	PCI_AD6	RESERVED
C8	IDE_DATA_S1	RESERVED	AA16	PCI_AD7	XBUS_D07
D8	IDE_DATA_S2	RESERVED	V16	PCI_AD8	XBUS_A19
B9	IDE_DATA_S3	TCK1	AB15	PCI_AD9	XBUS_A14
D9	IDE_DATA_S4	RESERVED	AA15	PCI_AD10	XBUS_A15
B10	IDE_DATA_S5	TMS1	Y15	PCI_AD11	XBUS_D06
E10	IDE_DATA_S6	RESERVED	W15	PCI_AD12	XBUS_A16
B11	IDE_DATA_S7	TDE1*	V15	PCI_AD13	XBUS_A17
A11	IDE_DATA_S8	TDE0*	AB14	PCI_AD14	XBUS_D04
E11	IDE_DATA_S9	RESERVED	AA14	PCI_AD15	XBUS_A13
C10	IDE_DATA_S10	RESERVED	Y11	PCI_AD16	XBUS_D03
E9	IDE_DATA_S11	RESERVED	W11	PCI_AD17	XBUS_CE*
A9	IDE_DATA_S12	TMS0	V11	PCI_AD18	XBUS_A12
C9	IDE_DATA_S13	RESERVED	AA10	PCI_AD19	XBUS_A9
E8	IDE_DATA_S14	RESERVED	Y10	PCI_AD20	XBUS_D02
AB	IDE_DATA_S15	TCK0	V10	PCI_AD21	XBUS_A10
E7	IDE_DRO_S	RESERVED	AB9	PCI_AD22	XBUS_A6
B6	IDE_INTR_S	TDI1	AA9	PCI_AD23	XBUS_D00
B7	IDE_IOR_S*	TD00	W9	PCI_AD24	XBUS_D01
C7	IDE_IOW_S*	RESERVED	V9	PCI_AD25	XBUS_A8
C6	IDE_RDY_S	RESERVED	AA8	PCI_AD26	XBUS_A3
			Y8	PCI_AD27	XBUS_A4
			W8	PCI_AD28	XBUS_A0
Y21	PCI_GNT0*	RESERVED	V8	PCI_AD29	XBUS_A5
Y18	PCI_GNT1*	RESERVED	V7	PCI_AD30	XBUS_A2
AA13	PCI_GNT2*	RESERVED	V6	PCI_AD31	XBUS_A1

BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME	BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME
Y7	PCI_GNT3*	RESERVED	Y16	PCI_CBE0*	XBUS_A18
Y6	PCI_GNT4*	RESERVED	W14	PCI_CBE1*	XBUS_DG5
V12	PCI_IRDY*	RESERVED	AA11	PCI_CBE2*	XBUS_A11
Y14	PCI_PAR	RESERVED	Y9	PCI_CBE3*	XBUS_A7
Y13	PCI_PERR*	RESERVED	Y12	PCI_DEVSEL*	RESERVED
AA20	PCI_REQ0*	RESERVED	AB11	PCI_FRAME*	RESERVED
AA18	PCI_REQ1*	RESERVED	V14	PCI_SERR*	RESERVED
AA12	PCI_REQ2*	RESERVED	V13	PCI_STOP*	RESERVED
AA7	PCI_REQ3*	RESERVED	W12	PCI_TRDY*	RESERVED
AA6	PCI_REQ4*	RESERVED			

VOLTAGE RAILS

RAIL	TYPICAL (V)	
V_CPUCORE	1.7V (CPU DEPENDENT)	
VCC	5V	
VCC3	3.3V	
V_SP0_STBY	5V STANDBY	
V_3P3_STBY	3.3V STANDBY	
V_2P5	2.65V	
V_1P5_VTT	1.5V	
V_1P25_MEMVTT	1.25V	
V_1P5	1.65V	
V_AGP_VDDQ	1.5V	
V_0P75_AGPUREF	0.75V	
V_1P0_CPUGTLREF	1.0V	

8	7	6	5	4	3	2	1	
*** Signal Cross-Reference *** --- For the entire design --- B_VREGULATED 41 40 I0_BIAS 35 I00_BIAS 35 AUD_SV_ANALOG 41 33 38 AUD_BCLK 36 23 AUD_BCLK_R 23 AUD_CK_24M 29 38 AUD_CK_24M_R 29 AUD_CLAMP 48 39 AUD_CLAMP_R 48 AUD_LINEOUT_L 48 43 AUD_LINEOUT_R 48 43 AUD_LINK_BCLK_CODEC_R 38 AUD_LINK_SDI1_CODEC_R 38 AUD_RST* 23 38 AUD_SDI0 38 23 AUD_SDI0 23 38 AUD_SYNC 23 38 AUD_TRANSIENT_CTRL 39 AUD_TR_CTRL_D1_P38 39 AUD_TR_CTRL_D2_P38 39 AUD_TR_CTRL_D2_P38 39 BGA2_BRC00_C5 6 BIAS_L 41 40 BIAS_R 41 40 CK_H_133M_CPU 11 6 CK_H_133M_CPU_BUF 6 CK_H_133M_CPU_R 6 CK_H_133M_FFB 11 CK_H_133M_FFB_R 11 CK_H_PICCLK 11 CK_H_PICCLK_R 11 6 CLK_XTAL_X1 29 CLK_XTAL_X2 29 CSYNC 12 46 CSYNC_L1 46 CSYNC_L2 46 CSYNC_L3 46 CSYNC_L4 46 DACA_Y 42 43 DACA_Y_F 42 DACB_C 42 43 DACB_C_F 42 DACC_SCART 42 43 DACC_SCART_F 42 DACD_CVBS 42 43 DACD_CVBS_F 42 DVEJECT 48 DVE_ACTIVE 48 DVO_ANALOG_VCC3 42 DVO_BLANK* 42 DVO_CLK0 42 12 DVO_CLK0R 42 DVO_CLK_IN 12 42 DVO_COMP 42 DVO_D<11..0> 12 13 42 DVO_DEFAULT 42 DVO_FIELD 42 12 29 DVO_FIELD_3P3* 23 DVO_FSADJ 42 DVO_FSADJ_R 42 DVO_HSYNC* 12 42 DVO_RESET_R* 42 DVO_VBIAS 42 DVO_VDD_VREFR 42 DVO_VREF 42 DVO_VSYNC* 12 42 EJECT_SW 48 EJECT_SW_R 48 FANFAN1 48 GREEN_LED 48 GREEN_LED_B 48 H0LR_PDD<15..0> 37 H_A*<31..3> 5 11 H_A20M* 24 5 H_A20M_R* 5 H_ADS* 6 11 H_BNR* 6 11 H_BRAT* 11 6 H_CPU_RST* 11 24 H_CPU_RST_R* 11 6 H_D*<63..0> 5 11 H_DBSY* 6 11 H_DEFER* 11 6 H_DRDY* 6 11 H_FERR* 5 24 H_HIT* 6 11 H_HITM* 6 11 H_LIGNNE* 24 5 H_INIT* 6 H_INTR 24 6 H_INTR_R 6 H_LOCK* 6 11 H_NMI 24 6 H_NMI_R 6 H_PREQ* 10 5 H_REQ*<4..0> 6 11 H_RS*<2..0> 11 6 H_SMI* 6 H_SMI_R* 24 6 H_TCK 10 5 H_TDI 10 5 H_THERMN 7 36 H_THERMP 36 7 H_TMS 10 5 H_TRDY* 11 6 H_TRST* 10 5 H_VID_0 26 H_VID_1 26 H_VID_2 26 H_VID_3 26 IDC_CSEL 37 IDC_IR014_R 37 IDC_PDA<2..0> 23 37 IDC_PDA_R<2..0> 37 IDC_PDCS1* 23 37 IDC_PDCS1_R* 37 IDC_PDCS3* 23 37 IDC_PDCS3_R* 23 37 IDC_PDD<15..0> 23 37 IDC_PDDACK* 23 37 IDC_PDDACK_R* 37 IDC_PDDREQ 37 23 IDC_PDDREQ_R 37 IDC_PDIO* 23 37 IDC_PDIO_R* 37 IDC_PDIO* 23 37 IDC_PDIO* 23 37 IDC_PINTR 37 23 IDC_PTORDY 37 23 IDC_PRI_RST_R* 37 KBRSTIN* 24 LAN_CK_25M 29 35 LAN_CK_25M_R 29 LAN_CLK_2_5M_RX 35 29 LAN_CLK_2_5M_RX_R 35 LAN_CLK_2_5M_TX 35 29 LAN_CLK_2_5M_TX_R 35 LAN_CT 35 36 LAN_CT_R 35 LAN_MII_COL 35 23 LAN_MII_CRS 35 23 LAN_MII_CRS_R 35 LAN_MII_RX_DV 35 23 LAN_MII_RX_DV_R 35 LAN_MII_RX_ER 35 23 LAN_MII_TX_EN 23 35 LAN_RD_N 36 35 LAN_RD_P 36 35 LAN_TD_N 35 36 LAN_TD_N_R 35 LAN_TD_P 35 36 LAN_TD_P_R 35 LDT_RESET* 12 24 LDT_RXD*<B..0> 24 12 LDT_RXD<B..0> 24 12 LDT_RX_CK 24 12 LDT_RX_CK* 24 12 LDT_TXD*<B..0> 12 24 LDT_TXD<B..0> 12 24 LDT_TX_CK 12 24 LDT_TX_CK* 12 24 LINE_OUT_L 38 40 LINE_OUT_R 38 40 LULCNT0 23 43 LULCNT1 23 42 43 L_AD<3..0> 23 25 L_FRAME* 23 L_SERIR0 23 MCPX_T0A0 24 25 MCPX_T0K1 24 25 MCPX_T0E0 24 25 MCPX_T0E1 24 25 MCPX_T0I0 24 25 MCPX_T0I1 24 25 MCPX_TMS0 24 25 MCPX_TMS1 24 25 MCPX_TRST1 24 25 MCP_3P3_DELAY 23 MCP_VDD_PLL 23 MII_MDC 23 35 MII_MDIO 23 35 MII_RXD<3..0> 35 23 MII_TXD<3..0> 35 23 MLAB_CKE 14 15 MLA_ADDR<13..0> 11 14 MLA_CAS* 11 14 MLA_CLK 11 14 MLA_CLK* 11 14 MLA_CS*<1..0> 11 14 MLA_DATA<31..0> 11 14 16 MLA_DOM<3..0> 11 18 14 MLA_DOS 11 14 16 MLA_RAS* 11 14 MLA_WE* 11 14 MLB_ADDR<13..0> 11 15 MLB_CAS* 11 15 MLB_CLK 11 15 MLB_CLK* 11 15 MLB_CS*<1..0> 11 15 MLB_DATA<31..0> 11 15 18 MLB_DOM<3..0> 11 18 15 MLB_DOS 11 15 18 MLB_RAS* 11 15 MLB_WE* 11 15 MLCD_CKE 16 17 MLC_ADDR<13..0> 12 16 MLC_CAS* 12 16 MLC_CLK 12 16 MLC_CLK* 12 16 MLC_CS*<1..0> 12 16 MLC_DATA<31..0> 12 16 19 MLC_DOM<3..0> 12 19 16 MLC_DOS 12 16 19 MLC_RAS* 12 16 MLC_WE* 12 16 MLD_ADDR<13..0> 12 17 MLD_CAS* 12 17 MLD_CLK 12 17 MLD_CLK* 12 17 MLD_CS*<1..0> 12 17 MLD_DATA<31..0> 12 17 19 MLD_DOM<3..0> 12 19 17 MLD_DOS 12 17 19 MLD_RAS* 12 17 MLD_WE* 12 17 ML_VREF_0 14 15 ML_VREF_1 16 17 30 NB_CK_13P3M 29 11 NB_CK_13P3M_R 29 NV2A_3P3_DELAY 12 NV2A_INTA* 12 24 NV2A_TEST 12 NV2A_VREF_0 11 NV2A_VREF_1 12 OUTPUT_CLAMP_L 39 40 OUTPUT_CLAMP_R 39 40 P0AC 35 36 P0AC_R 36 P1OL 35 36 P2LI 35 36 P2LI_R 36 P3TD 35 36 P4RD 35 36 PCI_CLK 24 23 PCI_CLK_FB 24 PCI_FRAME 24 25 PCI_PULLUP 23 24 PCI_RESET* 25 12 14 16 23 35 37 42 46 PCI_RESET_B* 24 25 PICD0 6 PICD1 6 PLLVDD 12 PLL_DELAY* 48 12 23 34 PLL_ENABLE 48 POWER_SW 48 POWER_SW_R 48 POWERON 32 29 48 POWERON 48 32 43 RED_LED 48 RGB_B 43 RGB_C 43 RGB_SELECT 43 RGB_SELECT* 23 43 ROM_A<19..0> 24 45 ROM_CE* 45 ROM_B<7..0> 24 45 ROM_OE* 24 45 ROM_OE_R* 45 ROM_WE* 24 45 ROM_WE_R* 45 RSET_NV2A* 12 RTC_DUMP 48 34 RTC_XI 23 RTC_XO 23								
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D	FB4P1 FERRITE 12	07F2 PNP 34	R2G10 RESN 48	R4R4 XRES 12						
	FB5A1 FERR_BD 40	07F3 PNP 34	R2G11 RESN 46	R4U1 RESN 30						
	FB5A2 FERR_BD 40	07G1 NPN 34	R2R1 RESN 26	R5A1 RESN 40						
	FB6C1 FERRITE 23	07N1 NPN 42	R2R2 RESN 26	R5A2 RESN 40						
	FB7A1 FERRITE 41	07R1 MBT3904DUAL 25	R2U1 RESN 26	R5A3 RESN 40						
	FB7A2 FERRITE 35	07U1 FET 34	R3A1 RESN 46	R5A4 RESN 40						
	FB8C1 FERRITE 29	08E1 FET 34	R3B1 RESN 48	R5A5 RESN 39						
	FP2G1 LPAK4L 46	08E2 NPN 28	R3B2 RESN 46	R5A6 RESN 39						
	FP5G1 LPAK4L 46	08E3 PNP 28	R3B3 RESN 48	R5A7 RESN 39						
	J1G1 2K5H0R 46	R1B1 RESN 10	R3B4 RESN 11	R5B1 RESN 39						
C	J2G1 1X12PWR 32	R1B2 RESN 10	R3B5 RESN 31	R5B2 RESN 48						
	J2G2 2K5H0R10 48	R1B3 RESN 10	R3C1 XRES 6	R5B3 RESN 48						
	J3A1 1X3H0R 46	R1C1 RESN 6	R3F1 RESN 30	R5B4 RESN 48						
	J4G1 2K5H0R 46	R1C2 RESN 6	R3F2 RESN 23	R5F1 RESN 16						
	J5A1 2AP_AV_BCC 43	R1C3 RESN 7	R3F3 RESN 23	R5F2 RESN 16						
	J6A1 1X3H0R 47	R1C4 RESN 7	R3G1 RESN 48	R5F3 RESN 16						
	J7D1 2K5H0R4 23	R1C5 RESN 6	R3G2 RESN 48	R5F4 RESN 16						
	J8A1 2K7H0R14 48	R1C6 RESN 6	R3G3 RESN 48	R5F5 RESN 16						
	J8C1 2K20H0R20 37	R1C7 RESN 7	R3G4 RESN 46	R5G1 RESN 46						
	JA7A1 RJ45_2LED_TABUP 36	R1C8 RESN 5	R3P1 RESN 11	R5G2 RESN 46						
B	L1F1 INDUCTOR 26	R1C9 RESN 6	R3P2 RESN 11	R5G3 RESN 46						
	L1G1 INDUCTOR 26	R1C10 RESN 7	R3R3 RESN 11	R5G4 RESN 46						
	L1R1 INDUCTOR 7	R1C11 RESN 5	R3R4 XRES 6	R5G5 RESN 46						
	L4A1 INDUCTOR 42	R1C12 RESN 6	R3R5 XRES 6	R5G6 RESN 46						
	L4A2 INDUCTOR 42	R1C13 RESN 5	R3R6 RESN 11	R5G7 RESN 46						
	L4A3 INDUCTOR 42	R1C14 RESN 6	R3U1 RESN 17	R5G8 RESN 46						
	L4A4 INDUCTOR 42	R1C15 RESN 6	R3U1 RESN 48	R5G9 RESN 31						
	L5G1 INDUCTOR 30	R1C16 RESN 6	R3U2 RESN 48	R5H5 RESN 40						
	L7F1 INDUCTOR 28	R1C19 RESN 6	R3U3 RESN 48	R5H6 RESN 41						
	L7G1 INDUCTOR 28	R1D1 RESN 7	R3U4 RESN 48	R5H7 RESN 41						
A	L7M1 INDUCTOR 36	R1D2 RESN 7	R4A1 RESN 48	R5H8 RESN 41						
	L7N1 INDUCTOR 36	R1D3 RESN 7	R4A2 RESN 42	R5H9 RESN 41						
	LB8D1 LABEL 44	R1D4 RESN 6	R4B1 RESN 42	R5H10 RESN 43						
	MTG1B1 MTGCONR_2_7 44	R1D5 RESN 7	R4B2 RESN 42	R5N1 RESN 41						
	MTG1E1 STD_MTG_EDGE 44	R1D6 RESN 6	R4B3 RESN 42	R5N2 RESN 40						
	MTG1F1 STD_MTG_EDGE 44	R1D7 RESN 7	R4B4 RESN 12	R5N3 RESN 41						
	MTG3A1 SLOT_X 48	R1D8 RESN 7	R4B5 RESN 13	R5N4 RESN 40						
	MTG3G1 SLOT_X 48	R1D9 RESN 6	R4B6 RESN 12	R5N5 RESN 41						
	MTG4B1 STD_MTG_HOLE 44	R1D10 RESN 6	R4B7 RESN 13	R5N7 RESN 12						
	MTG4E1 STD_MTG_HOLE 44	R1E1 RESN 26	R4B8 RESN 13	R5N8 RESN 12						
	MTG6F1 STD_MTG_HOLE 44	R1F1 RESN 26	R4B9 RESN 13	R5P3 XRES 11						
	MTG7C1 STD_MTG_HOLE 44	R1G1 RESN 46	R4B10 RESN 13	R5P4 XRES 11						
	MTG8A1 STD_MTG_HOLE 44	R1P1 RESN 7	R4B11 RESN 13	R5R1 RESN 12						
	MTG8G1 STD_MTG_HOLE 44	R1P2 RESN 5	R4B12 RESN 13	R6A1 RESN 40						
	Q1F1 FET_VREG 26	R1R1 RESN 26	R4B13 RESN 13	R6A2 RESN 25						
	Q2U1 FET_VREG 26	R1U1 RESN 26	R4F1 RESN 16	R6A3 RESN 40						
	Q2U1 PNP 48	R2B1 RESN 10	R4G1 RESN 30	R6A4 RESN 47						
	Q2U2 PNP 48	R2D1 RESN 6	R4G2 RESN 30	R6A5 RESN 43						
	Q3F1 FET_VREG 30	R2D2 RESN 26	R4G3 RESN 30	R6A6 RESN 43						
	Q3F2 NPN 23	R2D3 RESN 26	R4G4 RESN 30	R6B1 RESN 40						
	Q3N1 BCPS4 48	R2D4 RESN 26	R4G5 RESN 46	R6B2 RESN 38						
	Q4G1 FET_VREG 30	R2D5 RESN 26	R4G6 RESN 46	R6B3 RESN 40						
	Q5A1 NPN 39	R2D6 RESN 26	R4M3 RESN 42	R6B4 RESN 40						
	Q5A2 NPN 39	R2D7 RESN 26	R4M4 RESN 42	R6B5 RESN 38						
	Q5A3 NPN 39	R2E1 RESN 26	R4M5 RESN 42	R6B6 RESN 38						
	Q5A4 PNP 39	R2E2 RESN 26	R4M6 RESN 42	R6B7 RESN 38						
	Q5B1 MBT3904DUAL 48	R2E3 RESN 26	R4M7 RESN 42	R6B8 RESN 14						
	Q5F1 MBT3904DUAL 16	R2E4 RESN 26	R4N1 RESN 42	R6C1 RESN 14						
	Q5M2 NPN 41	R2E5 RESN 26	R4N2 RESN 42	R6C2 RESN 14						
	Q5N1 NPN 41	R2C6 RESN 26	R4N5 RESN 42	R6C3 RESN 14						
	Q5N2 FET 12	R2E7 RESN 26	R4N6 RESN 13	R6C4 RESN 14						
	Q5N3 FET 42	R2G1 RESN 46	R4N7 RESN 13	R6C5 RESN 14						
	Q6A1 PNP 43	R2G2 RESN 46	R4N8 RESN 13	R6C6 RESN 15						
	Q6C1 MBT3904DUAL 14	R2G3 RESN 46	R4N9 RESN 13	R6D1 XRES 23						
	Q6F1 FET 23	R2G4 RESN 46	R4N10 RESN 13	R6D3 XRES 24						
	Q7A1 NPN 47	R2G5 RESN 46	R4N11 RESN 13	R6E1 RESN 24						
	Q7A2 NPN 47	R2G6 RESN 46	R4N12 RESN 13	R6E2 RESN 23						
	Q7B1 PNP 47	R2G7 RESN 46	R4N13 RESN 13	R6E3 XRES 25						
	Q7E1 MBT3904DUAL 43	R2G8 RESN 46	R4R1 RESN 12	R6E4 XRES 25						
	Q7F1 FET_VREG 28	R2G9 RESN 48	R4R3 XRES 12	R6E5 XRES 25						
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FB8C1 FERRITE	29
FP2G1 LPAK4L	46
FP5G1 LPAK4L	46
J1G1 2X6HDR	46
J2G1 1X12PWR	32
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J5A1 2AP_AUL_BEC	43
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